

**From:** "Science Education Programs" <scienceeducationprog@orau.org>  
**Subject:** RISE Graduate Student Summer Internships with INTEL and HP  
**Date:** March 17, 2009 3:13:43 PM EDT  
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## **Research Internships in Science and Engineering Program Graduate Student Summer Internship Opportunities INTEL- India and HP-India**

Administered by ORAU

The Research Internship in Science and Engineering (RISE) is limited to the top U.S. students in a broad array of science and engineering disciplines. Each internship is from 3-6 months and all selected participants will receive housing (or housing allowance), roundtrip transportation to India, and monthly stipend. Eligibility is limited to US Citizens who are graduate students in science, technology, engineering or medical disciplines.

Twelve specific projects are listed below for HP-India and Intel-India. Students interested in the opportunities below should submit an application by March 27, 2009. Visit our website <http://rise.orau.org> for application and contact information. (Applications will also be accepted for other areas of research until the deadline.)

*Location: INTEL – Bangalore, India (2 Projects)*

- **Tera-Scale Platform**
  - ~ Silicon: On-die interconnect; cache architecture and dynamic reconfiguration; load scheduling on cores – perf & thermal; on-die power delivery ; BIST architectures and algorithms
  - ~ Package: MC / DRAM die-stack techniques ; packaging materials for high thermal loading ; dense I/O for MC packages ; cooling techniques and mathematical modeling
  - ~ Board and System: Topological implications of large fan-out from MC package ; System-level interconnect fabric ; resource partitioning architecture ; system security and trust models ; design of efficient power supplies and power delivery chains ; Transactional Memory HW architecture and support
  - ~ Software: New software models and architecture based on TM synchronization ; compiler techniques for Multi Core ; active partition management
  - ~ System on Chip (SOC)
- **Power Efficient Platform**
  - ~ Silicon: On-die Clock, On-die VR, Mesochronous Design Style, Design Tool implications
  - ~ Board and System: Support for Fine Grain Power Management, architecture and algorithms ; Low power fixed-function support structures e.g. streaming media processing ; high efficiency power delivery ; multi-radio management for interference and power reduction
  - ~ Low Cost Intel Architecture
  - ~ Low Power Intel Architecture

*Location: HP – India (10 projects)*

- **3-D hand pose estimation for gesture recognition:** Strong background in computer vision, image analysis and human-computer interaction is required.
- **A Type System based on Semantic Web:** Background in Programming Language design is essential. Exposure to Lambda Calculus, Type Systems required. Knowledge of logic programming and semantic web desirable.
- **Conversational multimodal interfaces:** Background in building dialog based/conversational interfaces for multimodal systems required.
- **Dynamic Network Analysis for Web Change analysis and modeling:** Knowledge of web mining, Graph algorithms is essential. Exposure to formal models, Dynamic Network Analysis will be an added advantage
- **Embedded P2P workflow engine:** Good knowledge of distributed systems, databases, embedded system and related topics. Good analytical skills and fluent programming ability in C++/Java are required. Background in middleware and web services would be ideal.
- **Gaze tracking:** Background in image processing, computer vision, pattern recognition etc. essential. Experience in building gaze tracking systems would be a plus

- **Human computer information retrieval:** Exposure to one of the following topics desirable - Relevance feedback, user intent determination/user profiling, faceted search, information visualization
- **Print and scan resilient semi supervised document clustering:** Image processing, pattern recognition and machine learning, C/C++, MATLAB, pursuing Masters or higher degrees in Electrical Engineering or Computer Science
- **Print-scan channel modeling and detection:** Strong base in digital communications, digital signal processing, Fourier transforms and related topics. Good mathematical skills and fluent programming ability in MATLAB/C are essential. Background in information and coding theory would be ideal.
- **User Action Understanding:** Exposure to sequence mining. Frequent pattern mining and related technologies, particularly in the context of web. Knowledge of some tools and techniques in Cognitive User Modeling will be of great advantage.

The Indo-U.S. Science and Technology Forum (IUSSTF) and Oak Ridge Associated Universities (ORAU) manage the RISE program. RISE provides opportunities for American graduate students to conduct research in India and for American institutions to host Indian graduate students and faculty in the U.S.

For more information, please contact:

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