Transistors: Field-effect transistors

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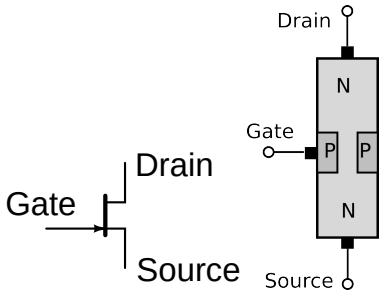
Week 8

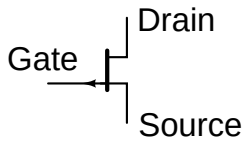
Field-effect transistor (FET)

Junction-FET

NJFET



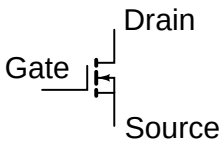
PJFET



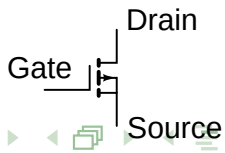
Metal-Oxide-Semiconductor FET (MOSFET)

- gate is truly isolated
- there is a forth terminal usually connected to source

NMOSFET



PMOSFET



FET vs BJT

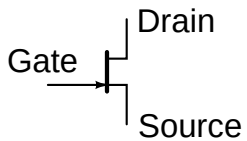
FET pros

- very high input impedance
  - JFET - impedance 10^{12} Ω
  - MOSFET - impedance 10^{14} Ω
- thus very small current into the base (pA range)
- can operate bidirectionally
- as result very little power consumption for the biasing network

FET cons

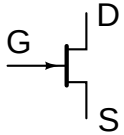
- have large parameter spread

Let's focus on NJFET

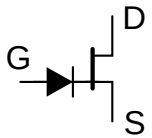


General notes

- N-channel usually faster due to higher mobility of electrons vs holes
- current goes from drain to source (thus the names)
- drain and source are nearly identical
  - thus sometimes gate is centered on some diagrams



  - can be used backwards with almost the same performance
- arrow indicates direction of the PN junction

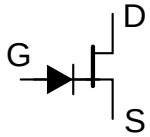


  - thus normal operation (low current into the gate) when $V_G < V_S$

NJFET gate voltage rules

V_p: pinch-off voltage (intrinsic parameter), $V_p < 0$ for NJFETs
it is called V_{th}:threshold voltage for MOSFETs

- $V_{gs} < V_p$
  - $I_D = 0$
- $V_{gs} > 0.6$ V
  - device fails, remember about gate diode



- $V_p < V_{gs} < 0.6$ V
  - normal operation
  - $I_d(V_{gs}, V_{ds})$

I_d vs V_{DS}

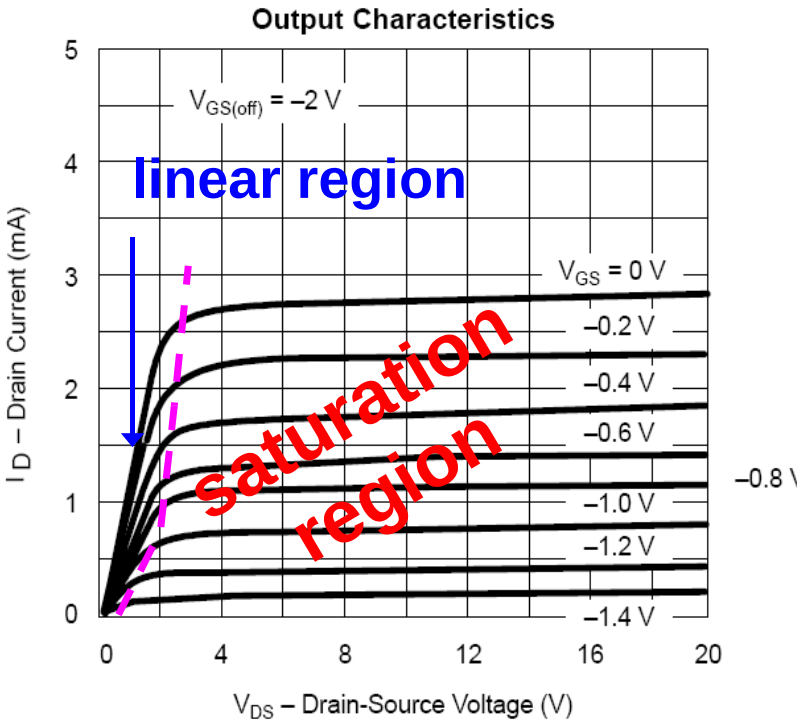
Linear region

- $V_{DS} < V_{GS} - V_p$
  - $Id(V_{DS}) = k(2(V_{GS} - V_p)V_{DS} - V_{DS}^2)$

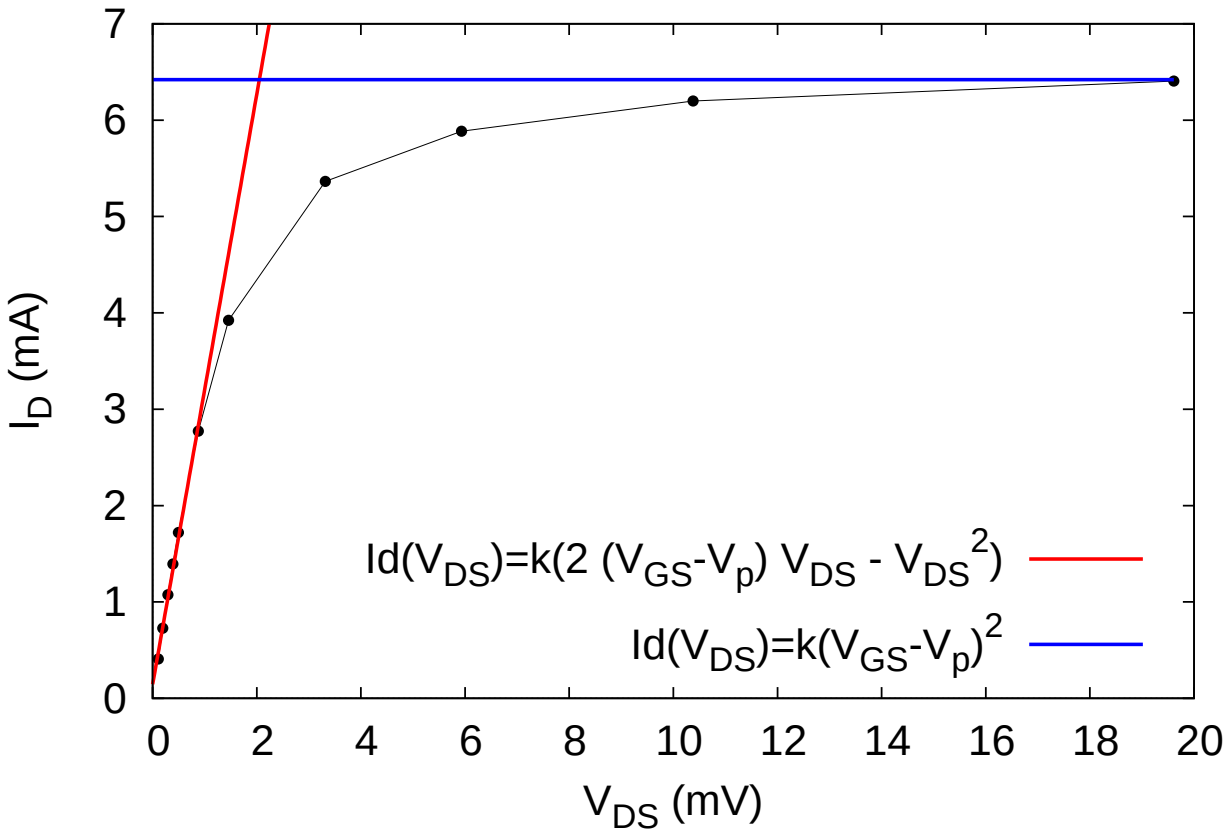
Saturation region

- $V_{DS} > V_{GS} - V_p$
  - $Id(V_{DS}) = k(V_{GS} - V_p)^2$

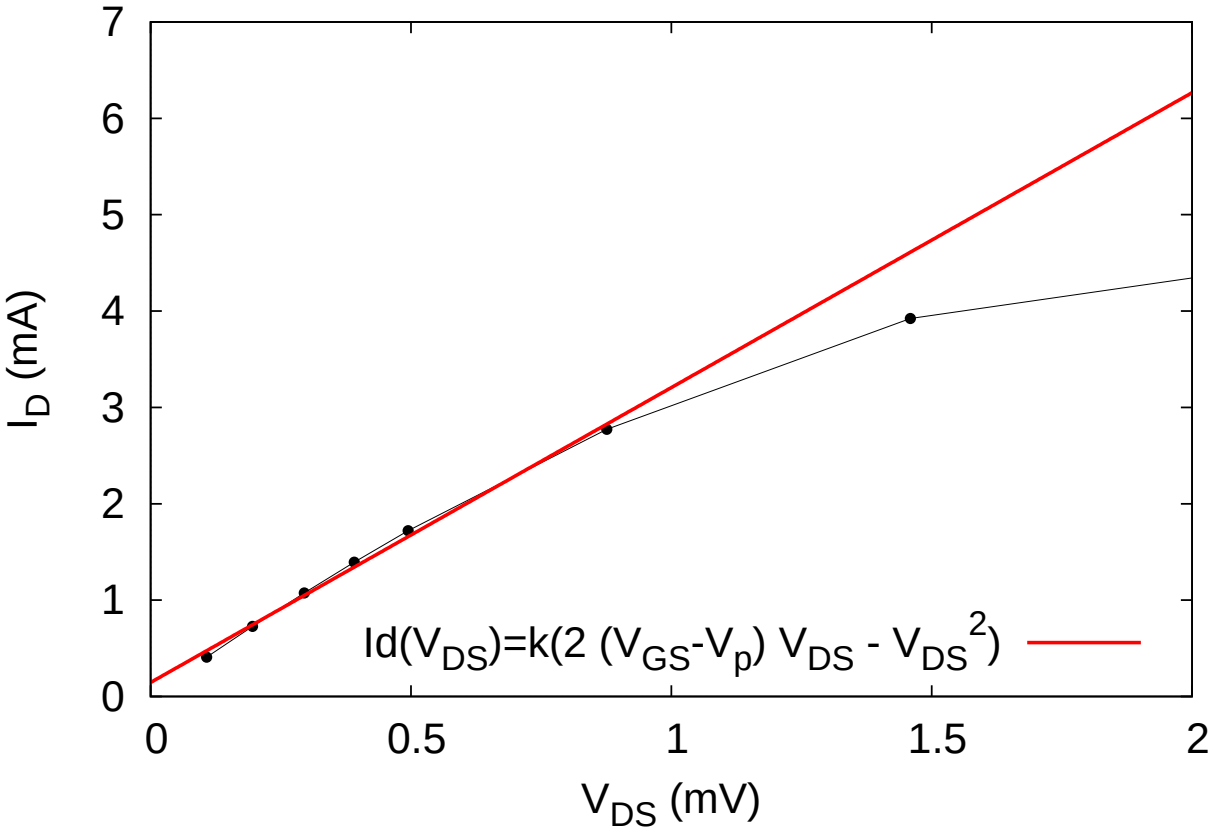
k is a constant



Real I_d vs V_{DS} linear region

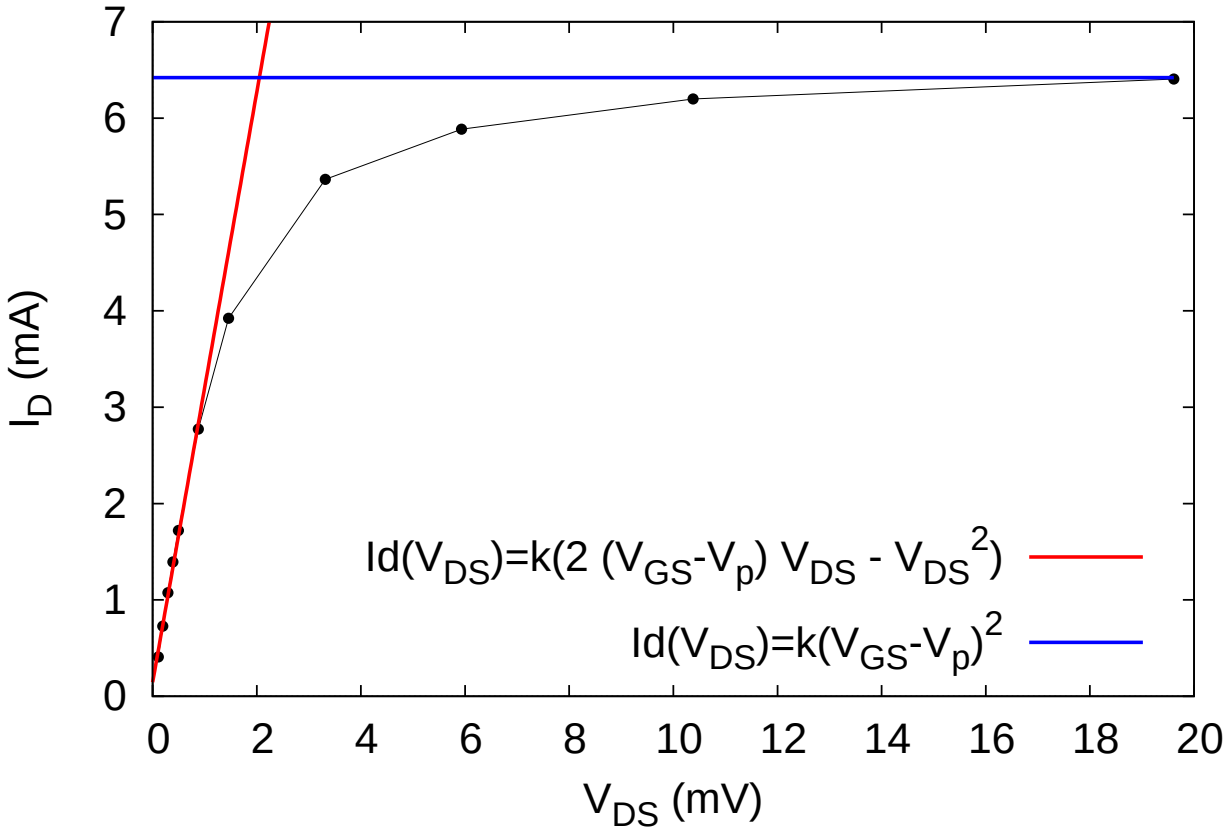


Real I_d vs V_{DS} linear region



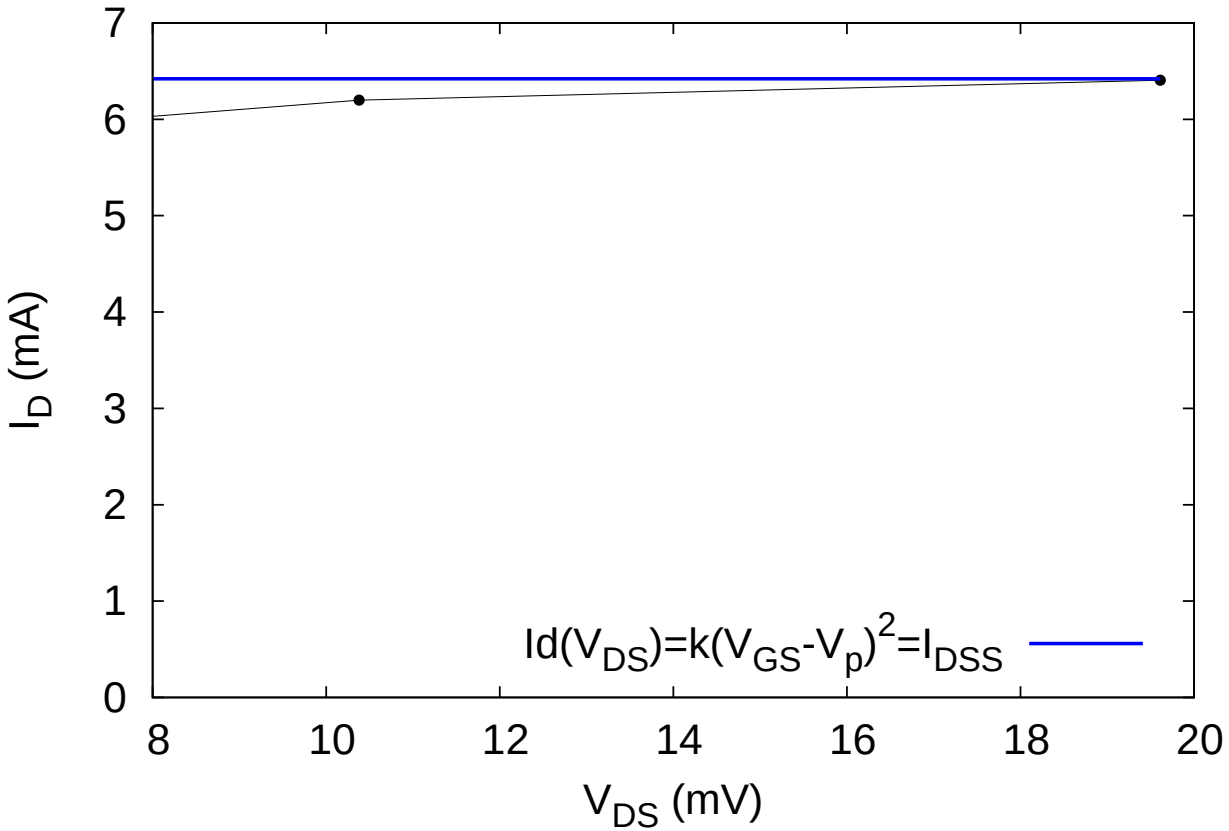
- $V_{DS} < V_{GS} - V_p$
  - $Id(V_{DS}) = k(2(V_{GS} - V_p)V_{DS} - V_{DS}^2) \approx 2k(V_{GS} - V_p)V_{DS}$

Real I_d vs V_{DS} saturation region



I_{DSS} saturation drain current, depends on V_{GS} and V_p

Real I_d vs V_{DS} saturation region



- $V_{DS} > V_{GS} - V_p$
  - $Id(V_{DS}) = k(V_{GS} - V_p)^2$

I_{DSS} saturation drain current, depends on V_{GS} and V_p

Reading the specifications

2N3958

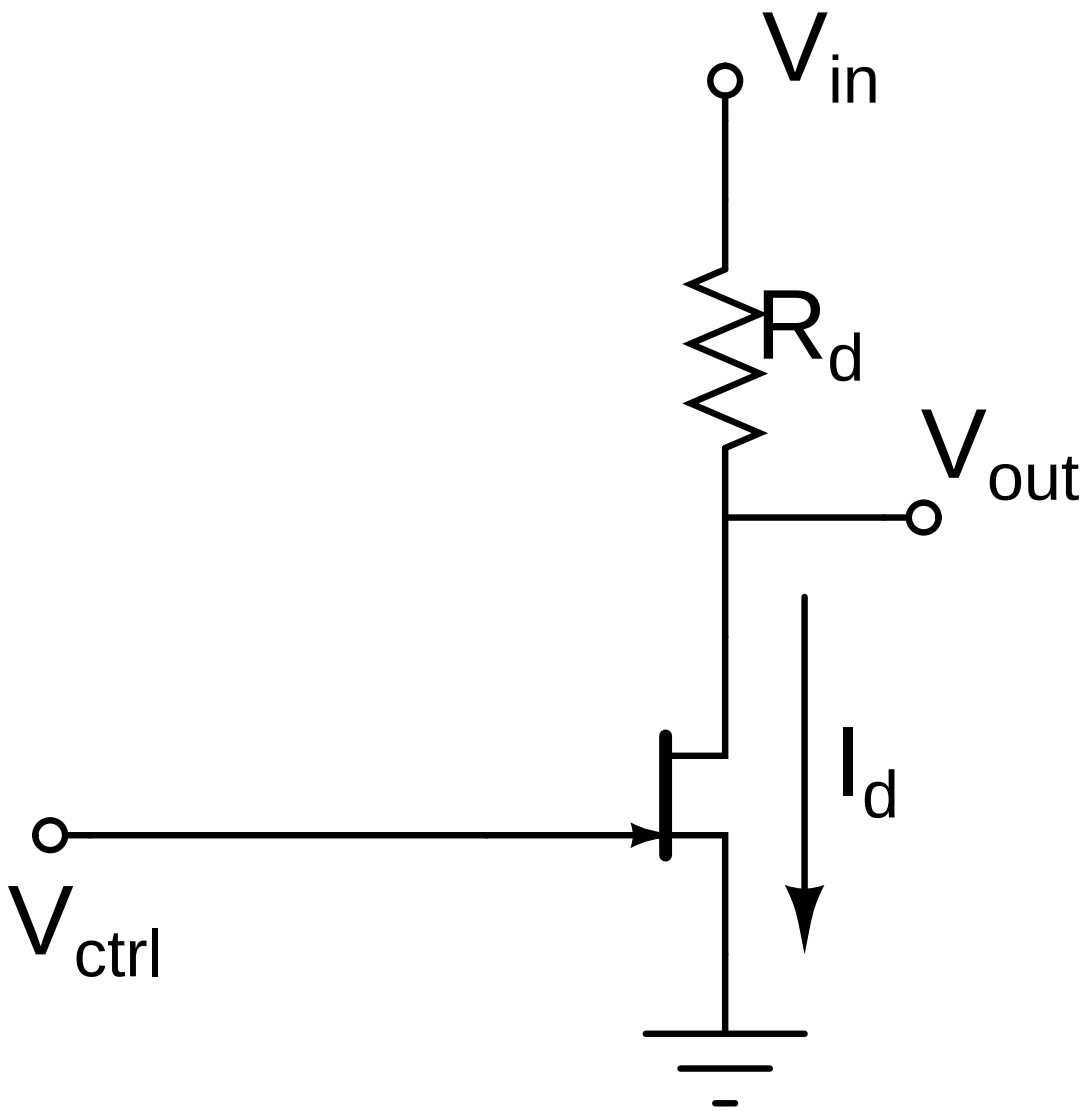
Vishay Siliconix

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

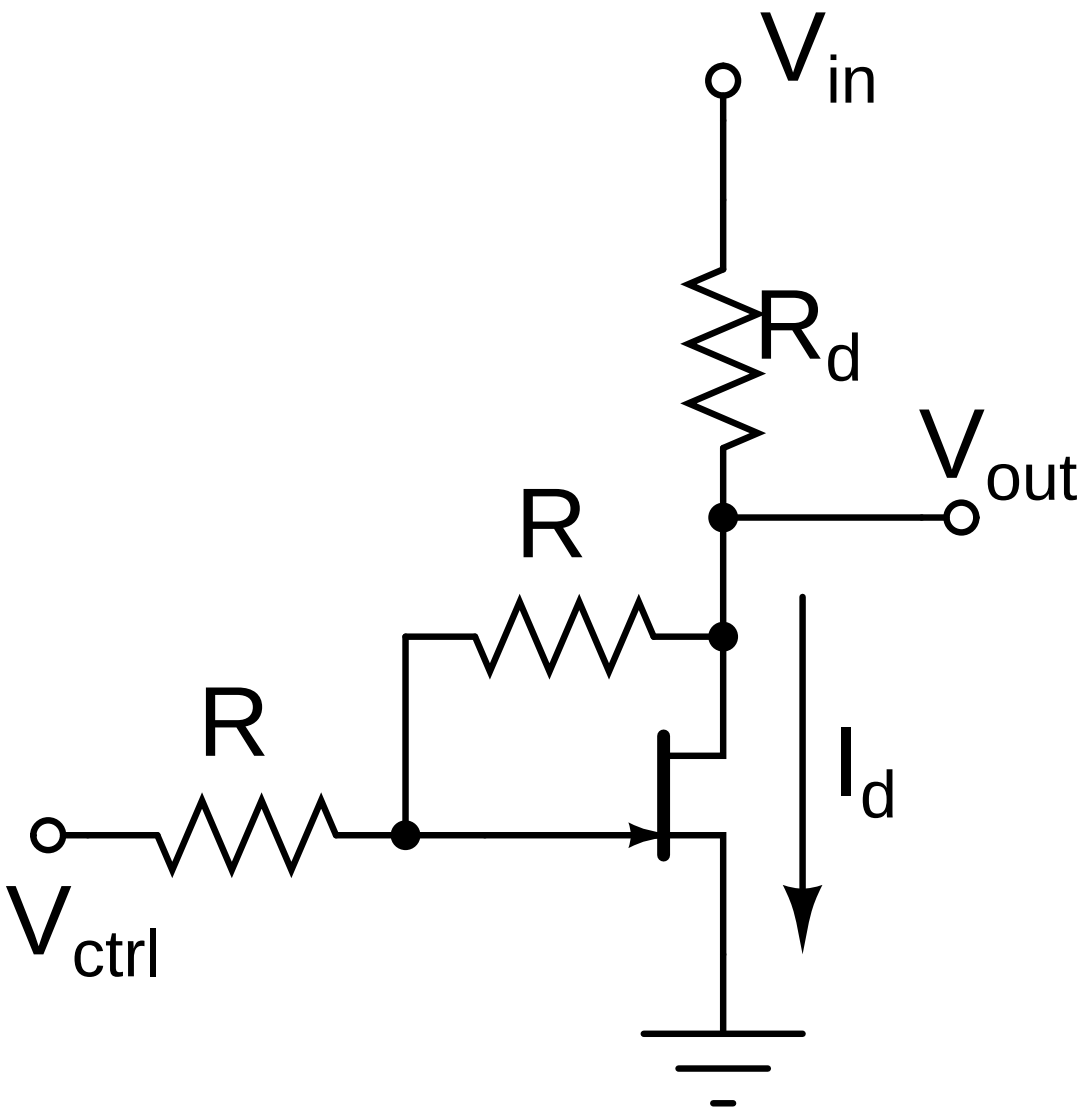
Parameter	Symbol	Test Conditions	Limits Min	Limits Typ[a]	Limits Max	Unit
Static						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 µA, V_{DS} = 0 V	–50	–57		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 20 V, I_D = 1 nA	–1.0	–2	–4.5	V
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	0.5	3	5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = –30 V, V_{DS} = 0 V		–10	–100	pA
		T_A = 150°C		–20	–500	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA		–5	–50	pA
		T_A =125°C		–0.8	–250	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA	–0.5	–1.5	–4	V
		I_D = 50 µA			–4.2	
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V			2	
Dynamic						
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	1	2.5	3	mS
Common-Source Output Conductance	g_{os}			2	35	µS

$V_{GS(off)}$ is the same as V_p

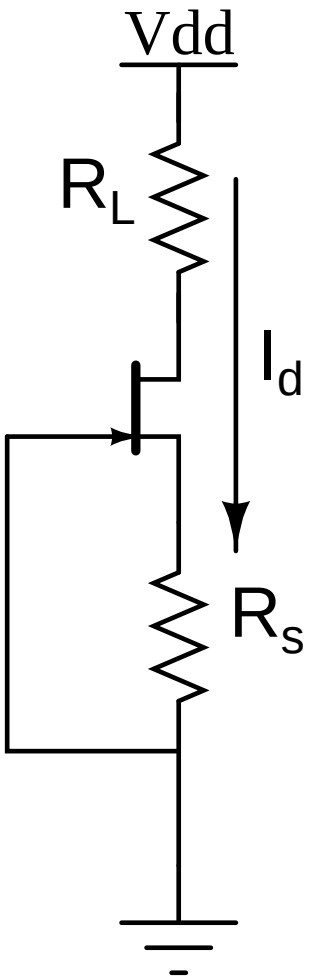
NJFET voltage controlled divider

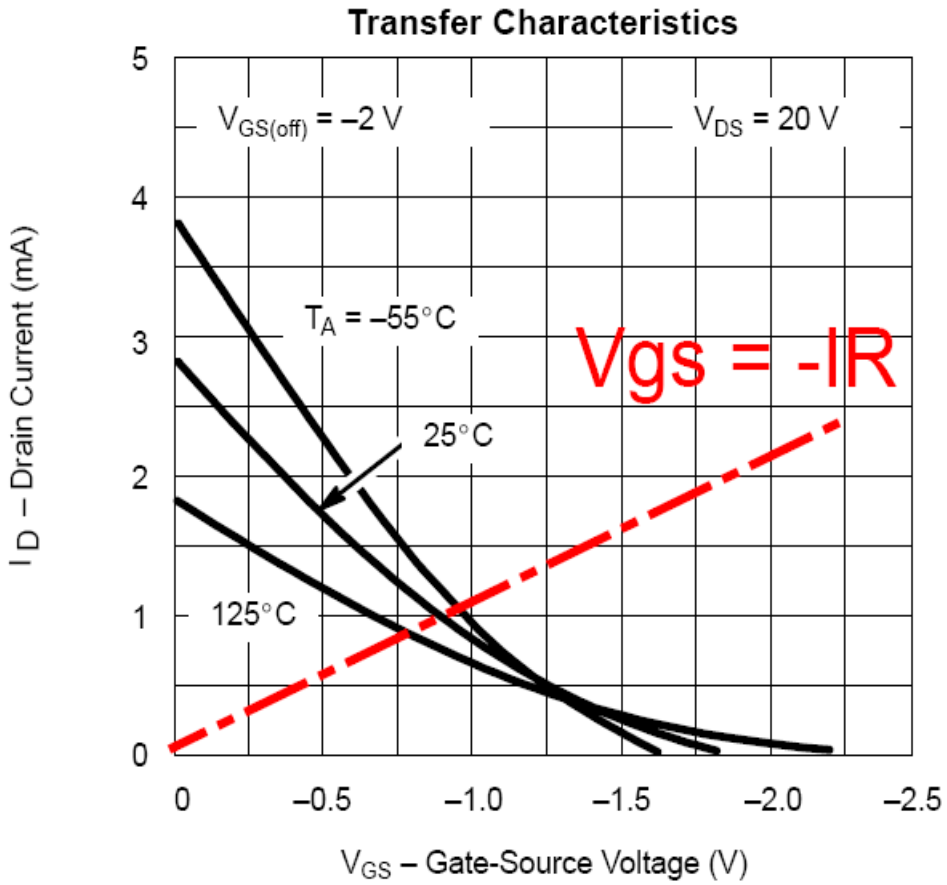


NJFET compensated voltage controlled divider

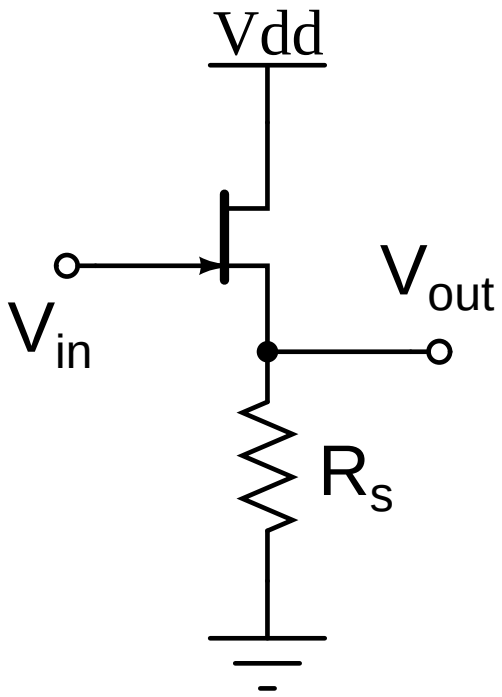


NJFET constant current source



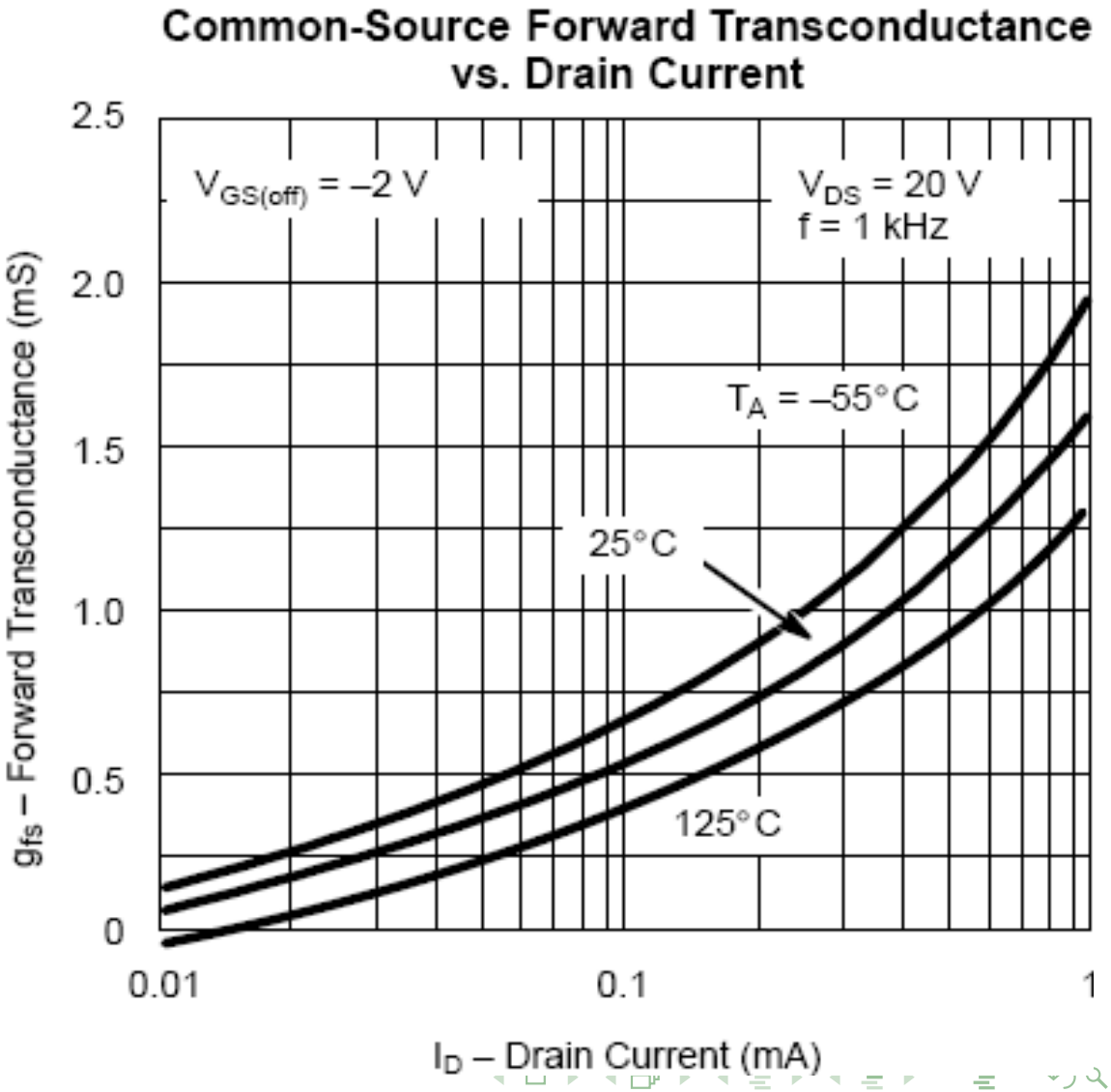


FET source follower

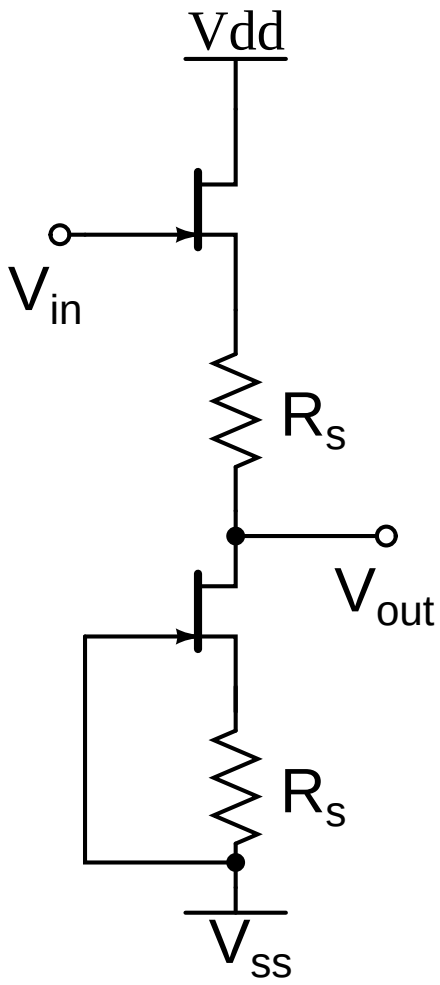


$$v_{out} = \frac{R_s}{R_s + 1/g_m} v_{in}$$

$$V_{out} > V_{in}$$



FET source follower improved



$$v_{out} = v_{in}$$

$$V_{out} = V_{in}$$