DESIGN EXERCISES – TRANSISTORS

i. *Voltage-Divider Bias circuit*

Design a VDB circuit that

- $R_1 \parallel R_2 < 0.1\beta_{dc}R_E$ (You can set beta=200 in Multisim)
- The current flowing through the voltage divider $I_{VD} < I_C$, preferably $I_{VD} < 0.1I_C$
- Emitter voltage $V_E \approx 0.1V_{CC}$
- About half of V_{CC} appear across the collector-emitter terminals: $V_{CE} \approx 0.5V_{CC}$
- You can decide a value of $V_{CC} = 10V \sim 15V$.

a) Show all the calculation below that how you picked the proper resistors to satisfy the design requirements above. Is your transistor working in the active region? Insert your simulation schematics below. (5)

b) Calculate $I_B, I_C \; and \; I_E$. Compare your calculation with simulation data. Display the three Volt/Ampere meters values in your simulation below. (5)

ii. VOLTAGE GAIN

a. Simulate this amplifier circuit below. Apply three Voltage meters: before C1 (v_{in}), before C2 (v_c) and after C2 (v_{out}). Insert your simulation below with graph. (5)

b. Calculate $I_E, r_c, r_e', A_{v,} \; v_{in} \; and \; v_{out}$. Note $v_{in} < v_g = 1mV_p$, but let's assume $v_{in} = 1mV_p$ Compare your calculation with your simulation graph. Insert your circuit and graph below. *If you read from the meters on the simulation, v_{pp} is peak-to-peak voltage while $1mv_p$ is peak voltage. Be careful.* (5)