THE COLLEGE OF WILLIAM AND MARY

Department of Physics

PORTABLE HIGH-FREQUENCY ULTRASOUND FOR SUBSURFACE CHARACTERIZATION OF MICROELECTRONICS

Christopher A. Houck

A thesis presented to the
Department of Physics of
The College of William and Mary
in partial fulfillment of the
requirements for the degree of
Bachelor of Science

May 2010

Williamsburg, Virginia

Portable High-Frequency Ultrasound for Subsurface Characterization of Microelectronics

Christopher A. Houck

May 2010

Abstract

Counterfeit, recycled, and maliciously modified integrated circuits (ICs) are a threat to information technology infrastructure. Delamination flaws in ICs present evidence that a chip has either been tampered with or modified. We have developed methods of introducing delamination flaws and detecting their presence through construction of a portable, high-frequency, contact, ultrasonic apparatus. We tested the ICs using high frequency ultrasonic transducers powered by an industrial PC equipped with an analog to digital board. We wrote programs in Matlab to process the signals and adapted the Dynamic Wavelet Fingerprint technique to decipher the data and discovered a repeatable pattern in the wavelet fingerprints for flawed and un-flawed ICs. We confirmed our results through immersion testing and imaging by means of ultrasonic C-scans

INTRODUCTION

Counterfeit, recycled, and maliciously modified integrated circuits (ICs) are a threat to the information technology (IT) infrastructure [1]. In 2006, The Alliance for Grey Market and Counterfeit Abatement (AGMA), an alliance of leading technology companies, estimated that 8% to 10% of all goods sold in the IT industry were counterfeit [2]. Counterfeit chips are easily acquired, either by finding discarded parts, or by stripping old ICs from circuit boards [3]. Electronics manufacturers purchase ICs from world-wide sources and through ever-changing supply chains, which increases the risk of attaining counterfeit parts. Counterfeit ICs increase the chance of electronic failure, which can be costly, and pose security threats, which can be deadly. It is of interest to develop low cost, easily executed methods to test ICs throughout the supply chain.

It is of paramount importance for manufacturers to detect the presence of counterfeit ICs early in assembly. ICs are relatively inexpensive compared to the electronic equipment of which they are components. It is estimated that the cost to find and repair a defect due to a counterfeit component increases ten-fold at every stage of assembly. For instance, if a defect is detected before installation the cost to repair is simply the cost of the IC. However, if the flaw is detected at the sub-assembly level the cost to repair is approximately 10 times the cost of the IC. At the customer level, the cost to find and repair the IC is 10,000 times the cost of the IC [2]. Consider the US Department of Defense's next generation F-35 Joint Strike Fighter which contains upwards of 1,000 chips. The difficulty of tracing a faulty chip back to its source, as well as the incredible cost of the damage that a malfunctioning chip could cause, is obvious [4].

The security threat posed by counterfeit chips is of great concern to the defense industry. In September of 2007, Israeli jets crossed the Syrian border and bombed a suspected nuclear target. The Syrian, state-of-the-art radar system mysteriously went dead, allowing the jets to cross unharmed. It has been speculated that microprocessor chips in the Syrian radar had been purposely manufactured with a kill-switch installed that could be triggered to cause momentary failure of the radar. Chips can be maliciously modified in a number of ways to cause the components to fail at a certain time, fail under a certain set of circumstances, or be triggered remotely to fail. Simply nicking a chip's copper wiring could cause a defense satellite to fail years before its expected life has expired [4].

Various methods of counterfeit flaw detection in ICs are already in use, but have considerable drawbacks. One method currently in use involves grinding thin layers of a chip away, then scanning the chip with an electron microscope [4]. The process must be repeated until the entirety of the chip has been scanned. This is a very labor intensive method that leaves the chip destroyed. X-rays are used to inspect chips; however, experienced technicians are required to effectively operate the X-ray machine. Acoustical microscopy is another common method of flaw detection, but this involves submerging the circuit board with the suspect chip which may damage the electronics [3].

We are developing a contact, high frequency ultrasound test apparatus/prototype to analyze the layers of ICs and detect flaws [5]. We are focused on detecting delamination flaws in the IC. Delamination flaws are commonly found in chips that have been stripped from old circuit boards. This is because the new, lead-free solders currently used have a higher melting point than the previously used lead-based solders.

When old chips are stripped from a circuit board, they are exposed to higher temperatures than they are suited for, resulting in delamination cracks. The test we are developing is relatively inexpensive and can be operated by an inexperienced technician.

Most ultrasonic flaw detection tests operate in the following manner. Ultrasonic pulses are generated by a piezoelectric transducer and transmitted into a sample by means of some coupling media. The pulse echoes are captured by the transducer and the time delay is recorded. Then computer analysis is used to decipher the recorded waveforms.

An ultrasonic transducer is a device that converts a voltage pulse into sound waves. *Figure 1* [21] displays the schematic of an ultrasonic transducer

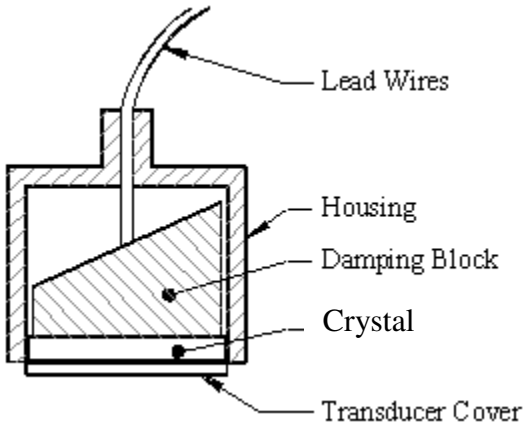


Figure 1: Schematic of an ultrasonic transducer. An alternating voltage pulse will cause the piezoelectric crystal to generate sound waves [21].

As a voltage pulse is applied, the piezoelectric crystal will change thickness at its resonant frequency and generate sound waves. A damping block is used to reduce the ring down time of the crystal and maximize axial resolution. A matching element is used to match the acoustic impedance of the crystal and probe delay to maximize wave transmission. The probe's ultrasonic energy must be coupled to the sample in some

manner as an ultrasonic transducer at MHz frequencies will not transmit waves through air due to the large impedance mismatch. Immersion testing is a common means of ultrasonic inspection. In this method, both the transducer and specimen are submerged, and water provides the coupling [6].

The transducer both propagates a signal and captures the returning pulse echo as illustrated by *Figure 2* [22].

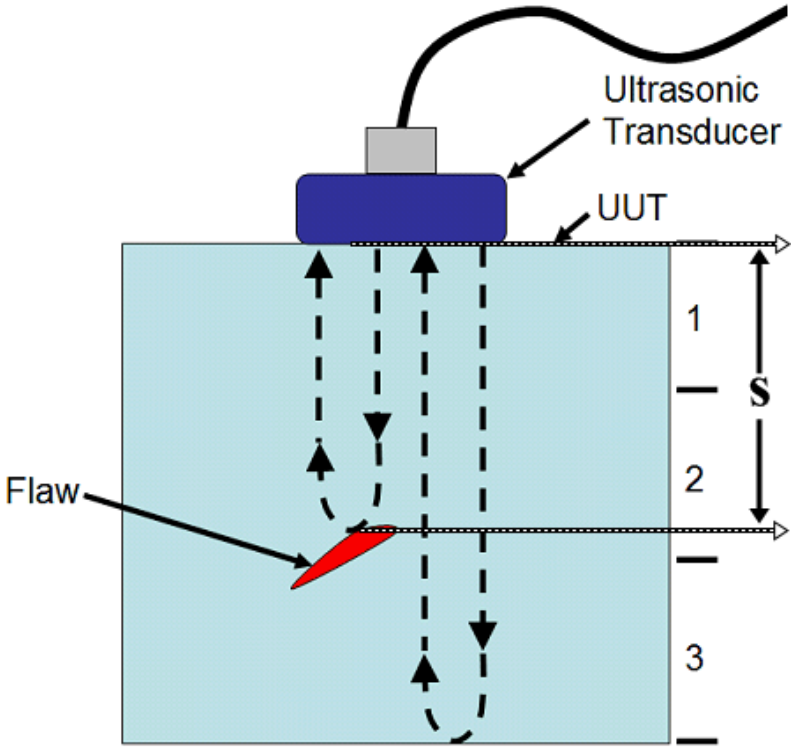


Figure 2: The ultrasonic transducer both propagates and captures a signal. The depth of the flaw (S) can be determined by knowing the velocity of sound in the sample and by measuring the time delay [22].

The depth of flaws can be determined by Equation 1.

$$s = \frac{ct}{2} \tag{1}$$

Here s is the distance between the crystal and the origin of an echo, c is velocity of sound in the specimen, and t is time. Features of the returning sound wave, such as amplitude

and location of peaks, are deciphered through analysis of waveform plots. Plots of pulse amplitude versus time (A-scan) can be generated by an oscilloscope or a computer with an analog to digital (A/D) board installed. The A/D board converts the physical ultrasonic pulse to digital values which are useful for signal processing. *Figure 3* displays a typical A-scan.

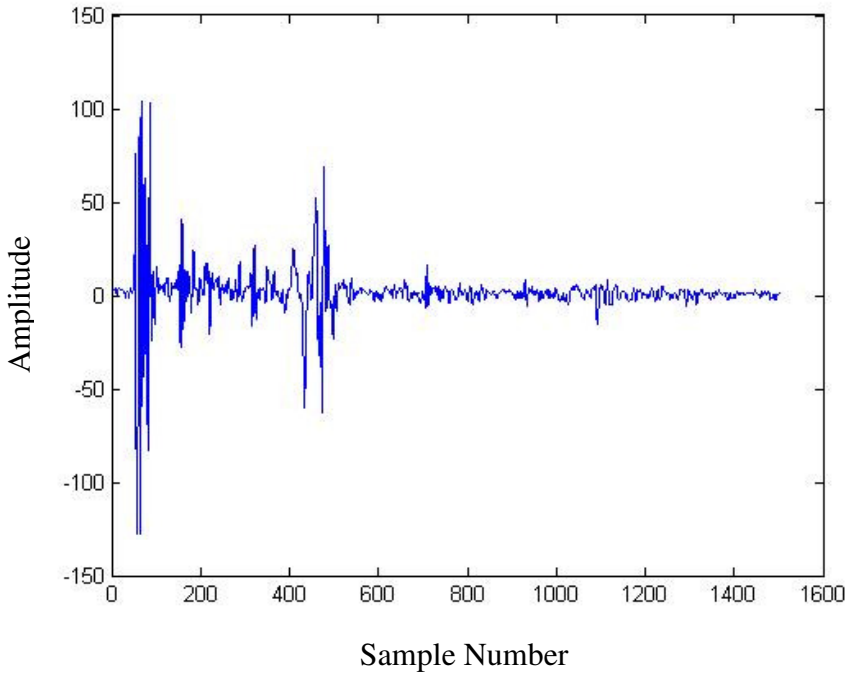


Figure 3: Typical A-scan. A plot of amplitude versus sample number for single waveform generated by an ultrasonic transducer. Sample number is a dimensionless value related to time. Sample number can be though of as the depth into a sample since distance is directly proportional to time.

A-scans display one waveform (or an average of multiple waveforms). In *Figure 2* amplitude vs. sample number is displayed. Sample number is a dimensionless value related to time, and thus distance, and is determined by the following equation:

$$sample\_number = \left(\frac{2d}{v}\right) sampling\_rate \qquad (2)$$

Here the sampling rate is the frequency that data is being collected, and $\frac{2d}{v}$ is the time it takes for the pulse to enter the sample and return to the transducer. Features of the sample are resolved through calculation and analysis. Samples can be imaged through a collection of many A-scans on an X-Y grid. This is called a C-scan. C-scans create images by displaying the depth of the sample's features across an X-Y plane. The amplitude of a feature at a given depth is indicated either by varying colors or shading as a colormap.

A-scans can be extremely difficult to decipher. The Dynamic Wavelet Fingerprint technique [7] has been found to be useful for a number of applications. *Figure 4* displays a sample we scanned with a handheld probe and the resulting A-scans from three different levels as well as their respective wavelet fingerprints.

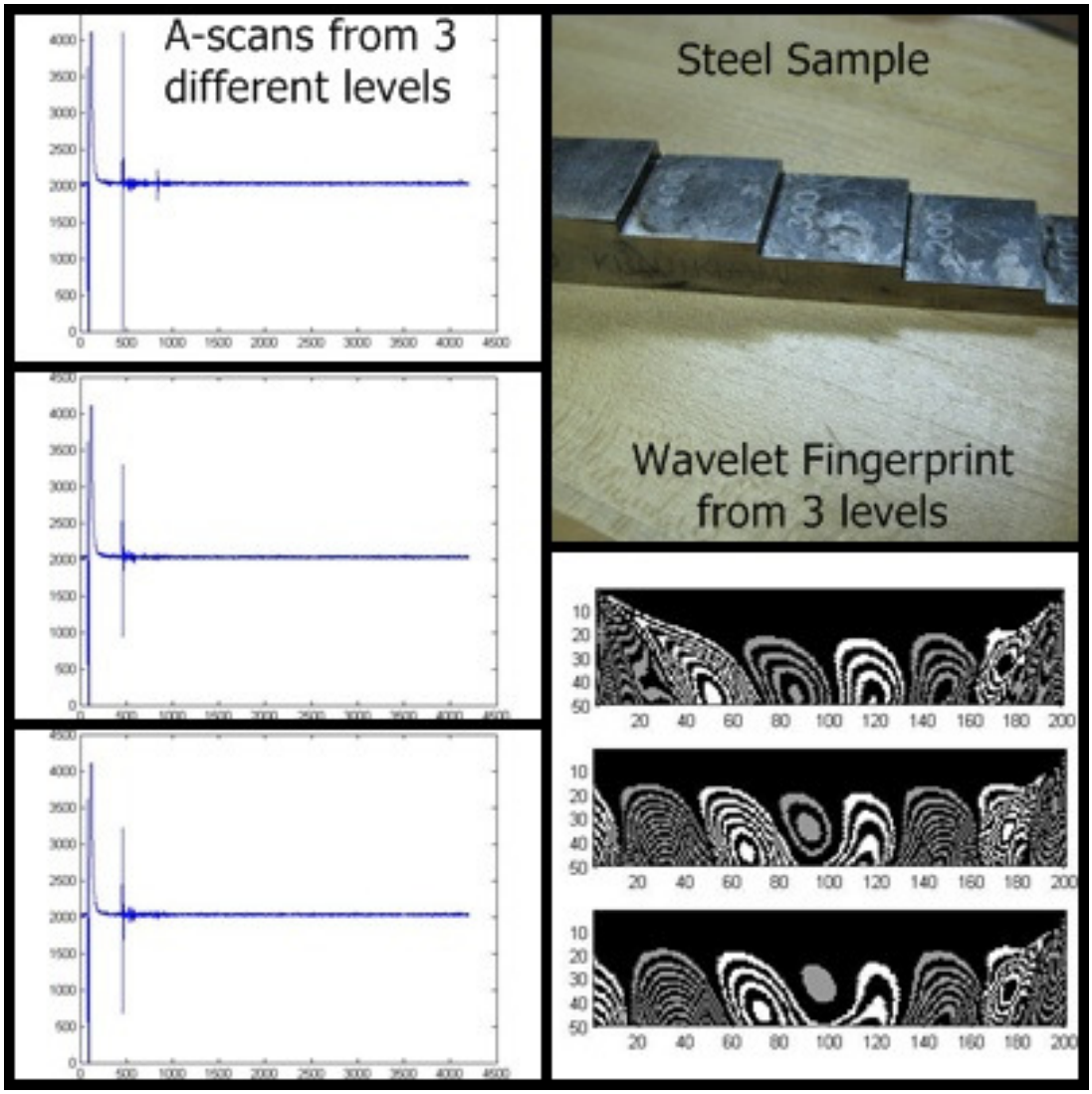
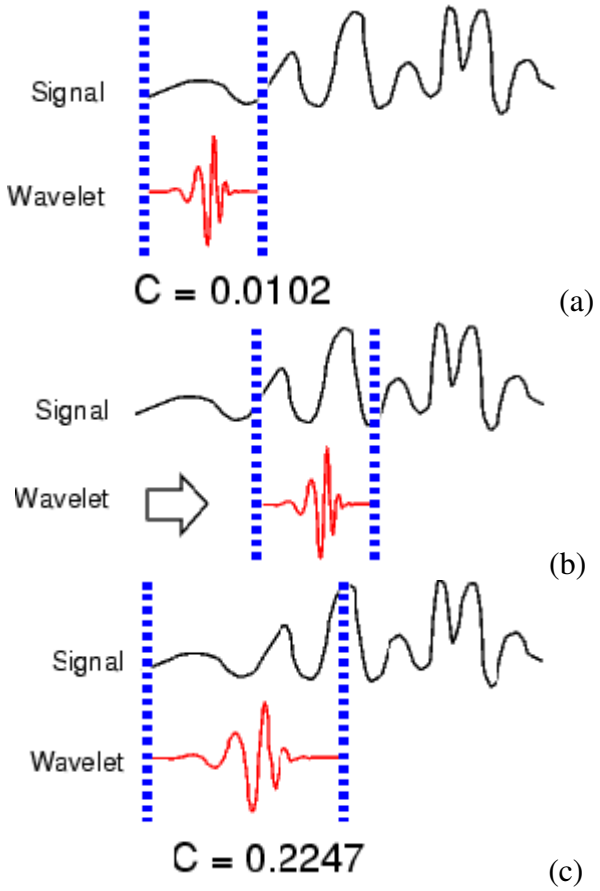


Figure 4: The steel sample was scanned by a handheld probe with the resulting three A-scans and corresponding wavelet fingerprints. Note the similarity between A-scans, and the obvious difference between wavelet fingerprints.

Note the similarity between A-scans, and the obvious difference between wavelet fingerprints.

The wavelet transform is similar to a short time-signal Fourier transform however; wavelet analysis relates scale to time, rather than frequency to time. This gives the wavelet transform a number of traits that are more desirable for signal processing such as determining when certain frequencies occur in a signal. It is also more flexible in

that wavelet functions can be customized for individual applications [7-18]. Scale essentially describes how compressed or stretched a wavelet is and is related to the inverse of frequency. A continuous wavelet transform is generated in the following method. The wavelet function is made up of parts containing different scaling factors where each part of the wavelet function is compared to the waveform at each instant in time. Correlation coefficients are generated for each part of the waveform. The coefficients range from -1 to +1 with the higher number reflecting a higher correlation. The resulting function gives a representation of the waveform. *Figure 5* demonstrates the process of generating coefficients for scales through time [19].



C = correlation coefficient; the greater the similarity between wavelet and waveform, the higher the correlation coefficient

Figure 5: Demonstrates a continuous wavelet transform. A wavelet is compared to the signal waveform (a) and a correlation coefficient, C, is generated at each moment in time (b). The process is repeated for different scales of the wavelet (c) [19].

This process allows 3-dimensional plots to be created reflecting the strength of correlation related to the scale factor and time as is demonstrated in *Figure 5 (b)* and is necessary step in wavelet fingerprinting. *Figure 6* displays how wavelet fingerprints are formed [7-18].

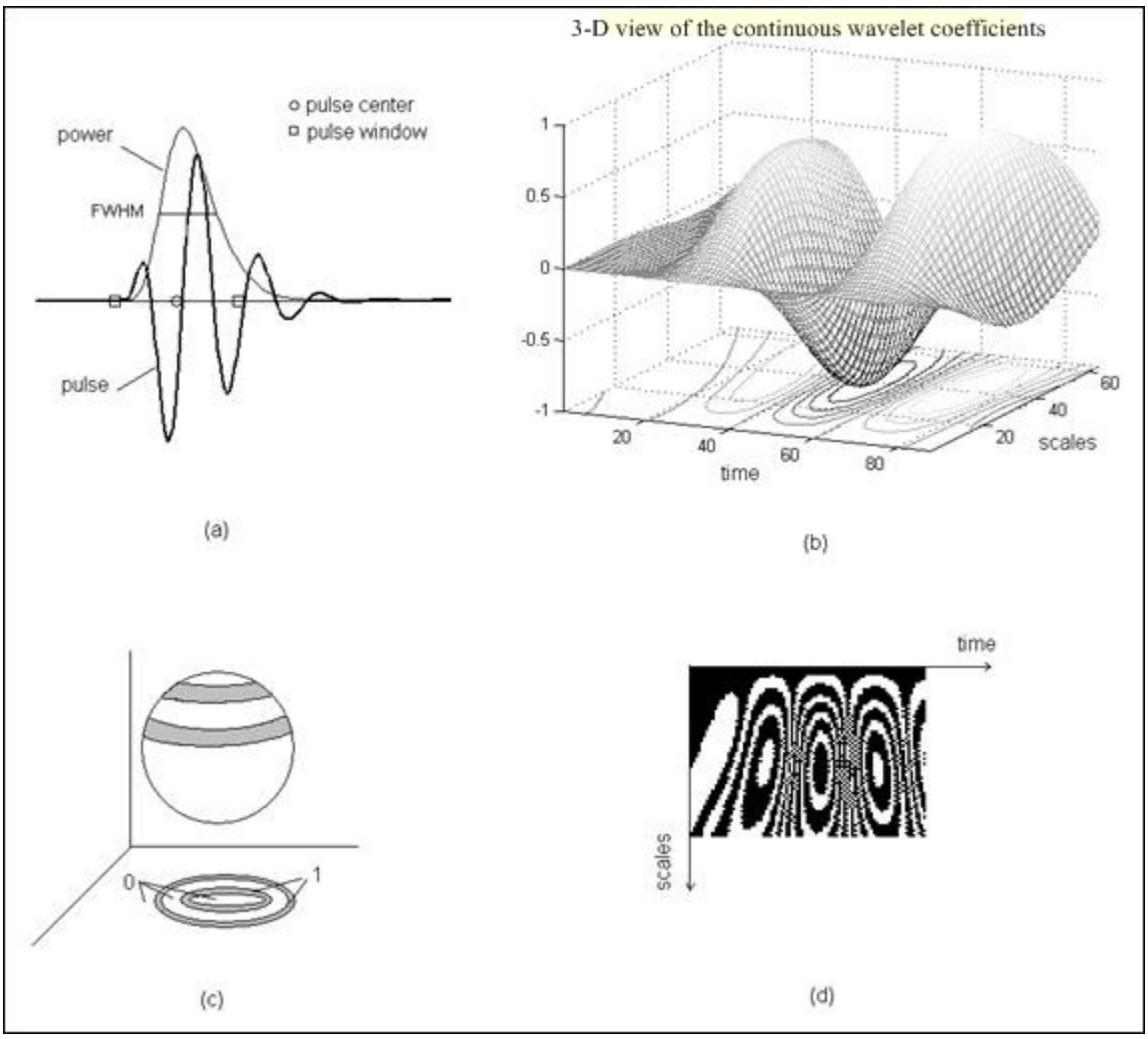


Figure 6: The process of generating wavelet fingerprints. A single waveform is recorded (a) and the continuous wavelet transform is implemented to generate a plot (b) relating the correlation coefficients to scale and time. Contour lines from the 3-D plot are transformed into a 2-D plot (c) which is the representation for wavelet fingerprints (d) [6].

A single waveform (a) is recorded. The continuous wavelet transform is implemented, plotting the wavelet coefficients on the z axis versus time and scale (b). In (c) the 3-dimensional contour lines are transformed onto a 2-D plot. This 2-D plot represents the wavelet fingerprint (d).

RESEARCH PLAN

Our first goal was to test and optimize a handpiece which contains a high frequency ultrasound transducer that couples the ultrasound signal into and back out of the chip surface in pulse-echo mode. The second was to assemble a benchtop ultrasound apparatus that acquires pulse-echo data using a portable computer running Matlab. The third was to adapt our existing Dynamic Wavelet Fingerprint algorithms to help distinguish between good and bad ICs.

These tasks are accompanied by multiple technological challenges. The first is the difficulty in coupling a high frequency transducer directly with the sample. This is simple at low frequencies, but at 100MHz any small gap or misalignment will ruin the signal. Also, the attenuation of ultrasonic pulses increases with the square of the frequency. This can make it difficult to locate flaws deep within a sample. Another challenge is in creating advanced signal processing that requires little analysis by the user. The signal processing should be sophisticated enough to automatically detect flaws without requiring advanced training for the user.

Our research is concentrated in three areas: flaw introduction, apparatus construction, and flaw detection. We are focused on delamination flaws in ICs. Delamination occurs when the small gaps in an IC pick up moisture. The moisture can expand when heated and cause cracks. These types of defects are often found in counterfeit ICs that have been stripped from old boards and re-soldered onto a new board. Older chips were soldered to boards with a lead solder that has a lower melting point than the solder currently used. Thus, when the ICs are re-soldered, they are subject to a higher

temperature than they are suited for, and cracks can occur. These cracks, or delaminations, are a result of what is known as the "popcorn effect" [5].

We have developed a process to introduce delamination flaws by constructing a misting chamber that creates a very humid (85% relative humidity) and warm environment (80°C). ICs are inserted into the chamber for a week. See *Figure 7*.

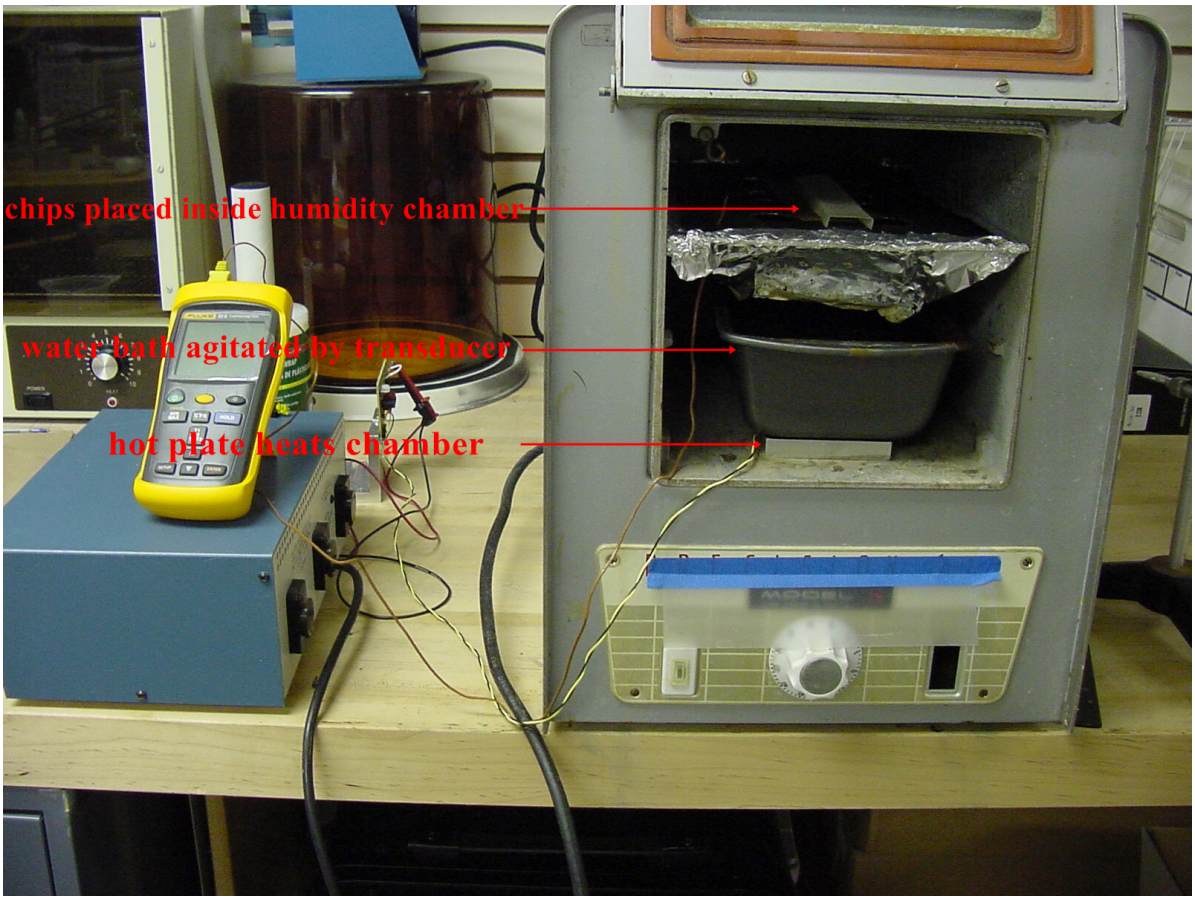


Figure 7: Misting chamber. IC's were inserted into the chamber for a week and were subjected to a very warm, humid climate.

Upon their removal, we subject the ICs to a reflow profile designed to simulate the shock of soldering where the chips reach a temperature of 260°C in a matter of minutes. We used a hot-air lamp and a PID controller for this process. See *Figure 8*.

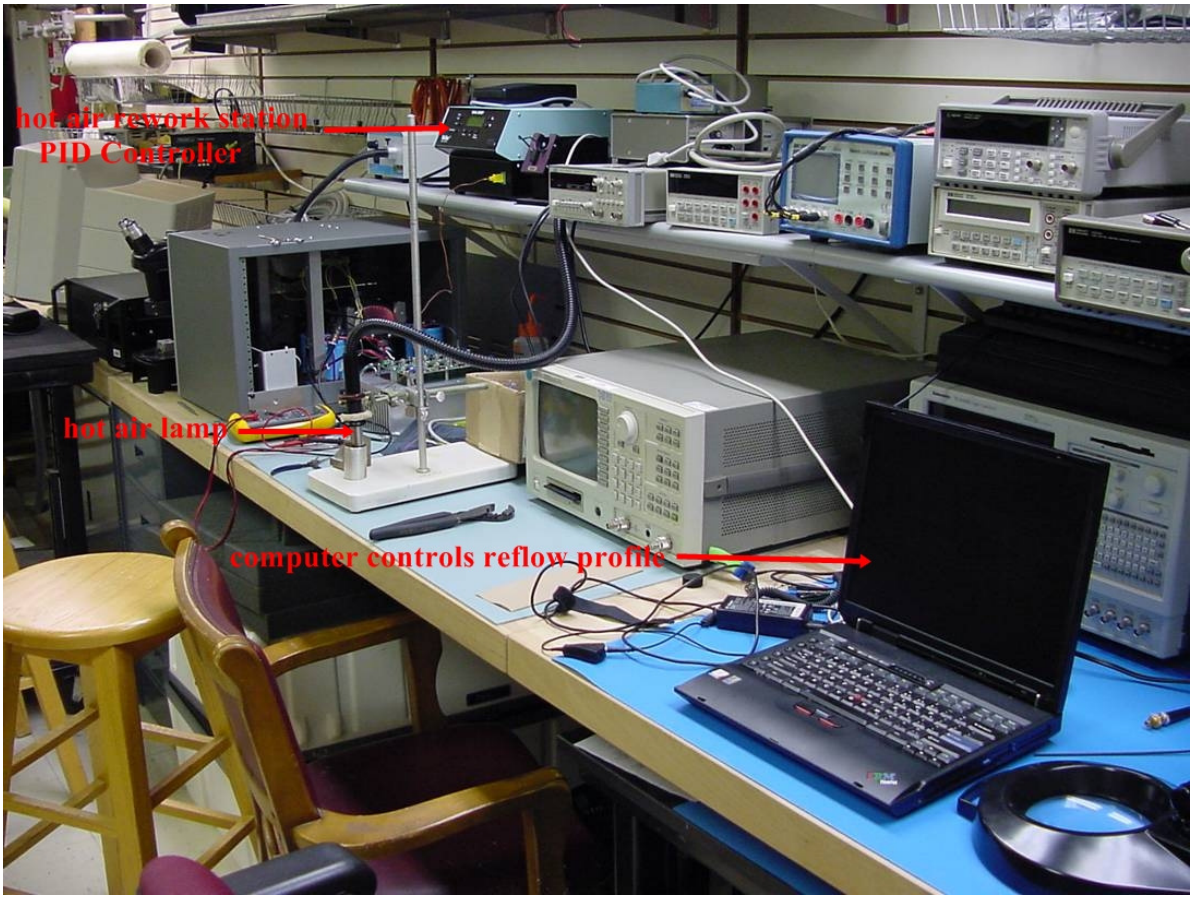


Figure 8: Reflow profile apparatus. Computer controls hot air lamp, which heats IC's to 260°C to simulate the shock of soldering.

We have also developed and assembled the necessary components to take data. The base of our benchtop apparatus is an industrial PC with the necessary A/D and ultrasonics cards installed. The ultrasonic pulser-receiver card sends a voltage pulse to a 100MHz transducer. A tapered quartz delay line is fixed to the transducer to minimize its footprint on the ICs. A drop of oil based liquid is used as a couplant between the delay line and the IC. We made a damping jacket out of shrink-wrap for the delay line. It is lined with the couplant so as to minimize noise arising from the pulse reflecting off the walls of the delay line. We machined a stabilizer arm to hold the transducer. The

stabilizer arm helps maintain the transducer at the correct orientation while allowing freehand movement.

The transducer both propagates and captures the pulse. We have written a number of programs in Matlab to process the signal received from the transducer and have developed a graphical user interface (GUI) to save the A-scans. Another program was written to apply the wavelet transform to each A-scan and display the results. We can modify the type of wavelet family used for the transform and can toggle numerous constraints to optimize the results. *Figure 9* displays the data collection apparatus.

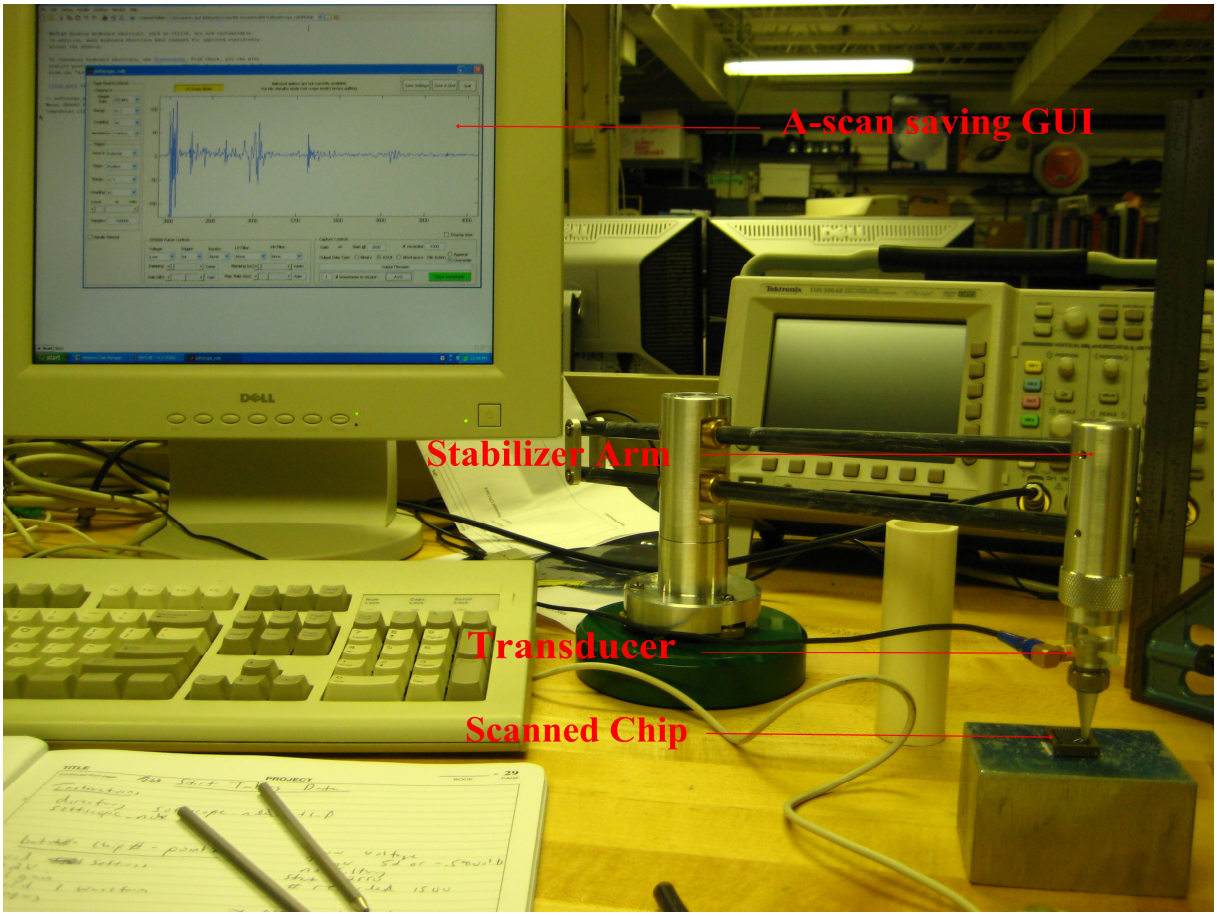


Figure 9: The data collection apparatus. The monitor displays the A-scan saving GUI. The transducer/delay line unit is held by the stabilizer arm while it scans a sample.

The monitor displays the A-scan saving GUI. The transducer/delay line unit is held by the stabilizer arm while it scans a sample.

RESULTS FROM 100MHZ TRANSDUCER

We subjected approximately 12 of both 32 pin PLCC ICs and 12 thinner 56 pin TSOP ICs to the misting chamber and reflow profile, *Figure 10*.

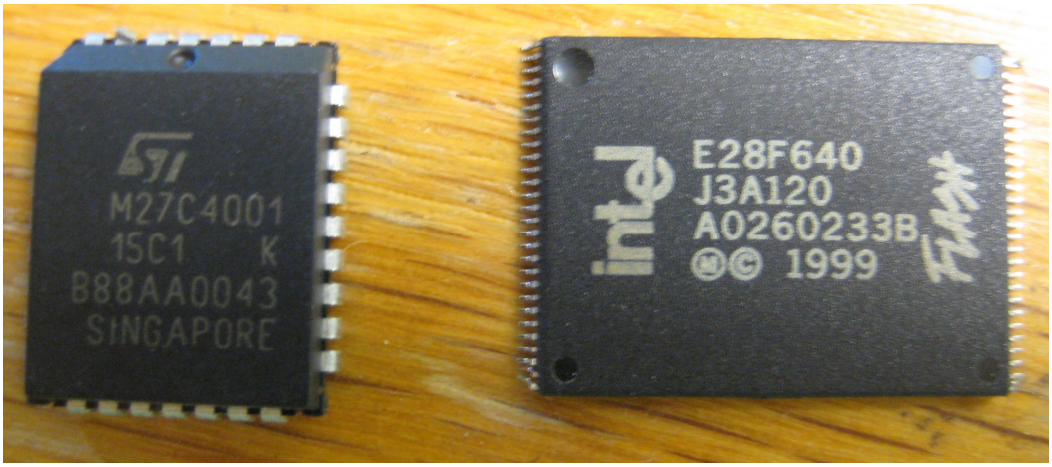


Figure 10: Integrated circuits we performed our research on. We scanned 12, 32 pin PLCCs (pictured left) and 12, 56 pin TSOPs (pictured right)

Visible delamination flaws were noted on the back face of five different 56 pin chips. The rest of the ICs may or may not be flawed. We collected 48 waveforms on the 56 pin chips and 30 on the 32 pin chips using a 100MHz transducer. Data was collected in an approximate grid; however, positioning was freehand because we were specifically not trying to image the chip. All of the ICs subjected to the misting chamber and reflow profile were scanned as well as three controls of both types. Three different users scanned data to help determine inter-operator variability.

We extensively analyzed the data to determine a repeatable pattern in the wavelet fingerprints for the control chips and for the flawed chips, however, there was no

consistent pattern using the 100MHz transducer. We examined the shapes of the prints, the number of rings, the number of prints, and the location of the prints with respect to time. We expected to see something similar to *Figure* 4, where a different number of rings differentiates the features of the sample. The following figures display examples of our data.

Figure 11: Displays wavelet fingerprints of 48 waveforms taken from a TSOP IC using a "dmey" filtering wavelet and a "db3" wavelet transform and 100MHz transducer.

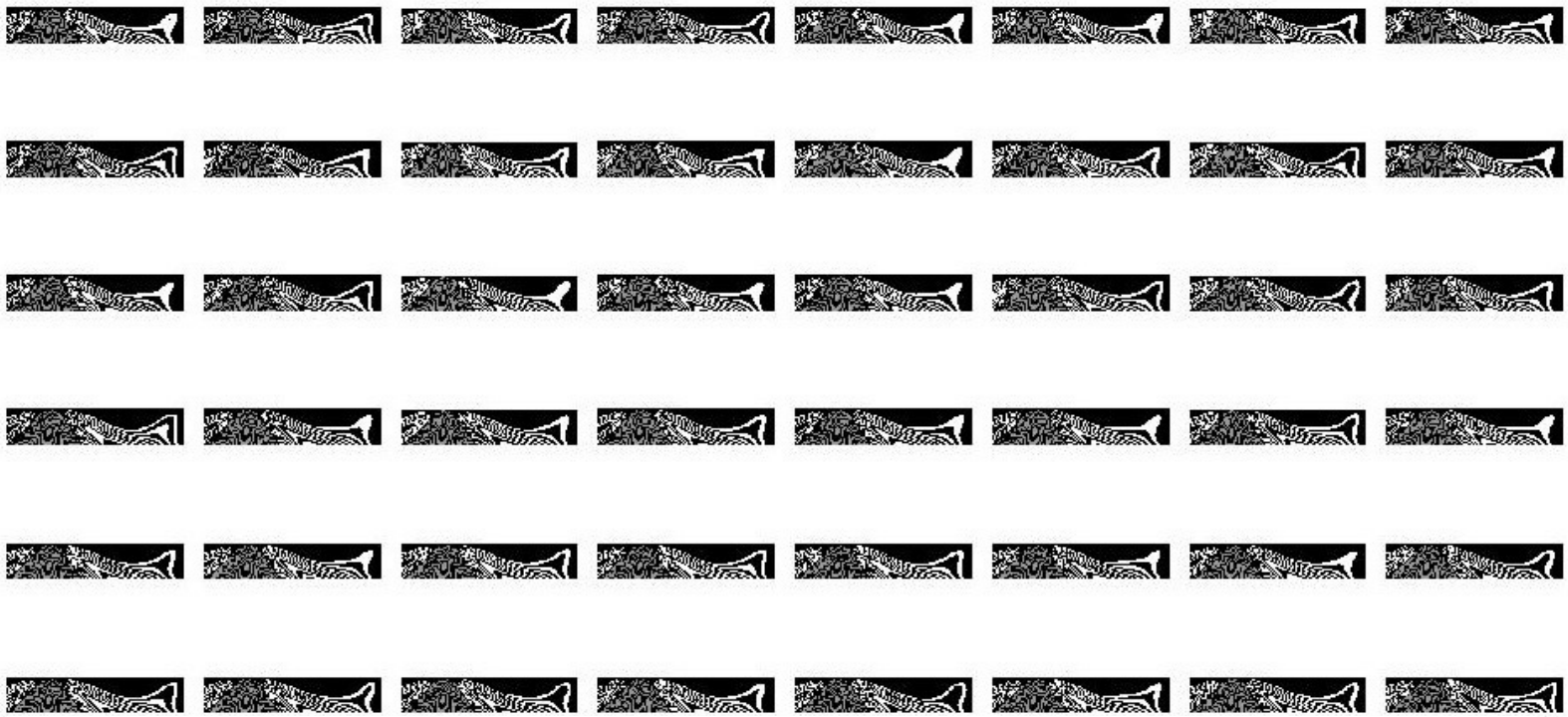


Figure 12: Displays fingerprints from the same chip as Figure 11 with a different transform applied. A "haar" filtering wavelet and a "mexh" wavelet transform were applied.

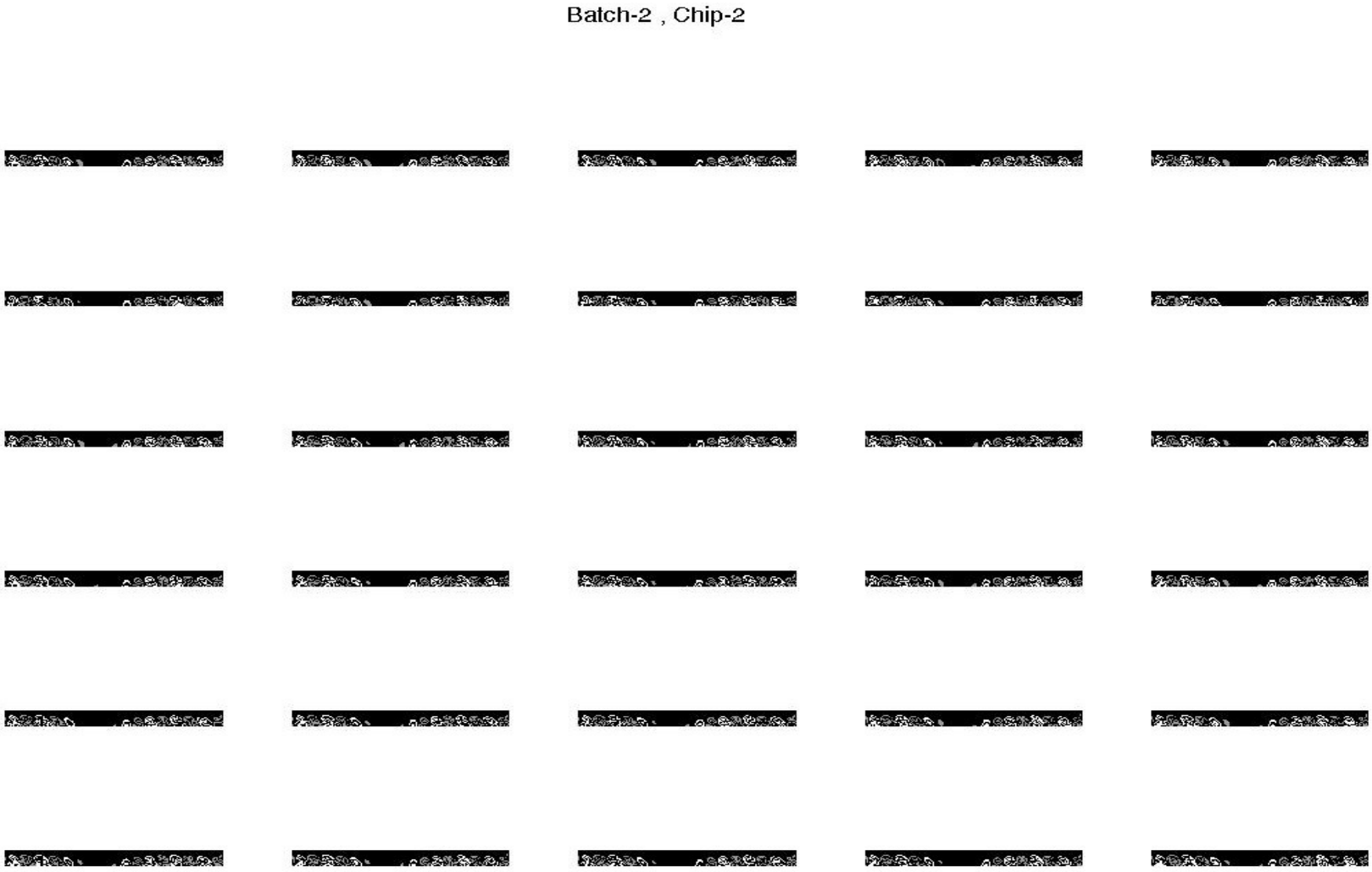


Figure 13: Displays wavelet fingerprints of 30 waveforms taken from a PLCC IC using a "dmey" filtering wavelet and a "db3" wavelet transform and 100MHz transducer.

Figure 14 explains the meaning of the wavelet abbreviations [19].

Wavelet Family Short Name	Wavelet Family Name
'haar'	Haar wavelet
'db'	Daubechies wavelets
'sym'	Symlets
'coif'	Coiflets
'bior'	Biorthogonal wavelets
'rbio'	Reverse biorthogonal wavelets
'meyr'	Meyer wavelet
'dmey'	Discrete approximation of Meyer wavelet
'gaus'	Gaussian wavelets
'mexh'	Mexican hat wavelet
'morl'	Morlet wavelet
'cgau'	Complex Gaussian wavelets
'shan'	Shannon wavelets
'fbsp'	Frequency B-Spline wavelets
'cmor'	Complex Morlet wavelets

Figure 14: Displays the wavelet families along with their respective abbreviations.

Each wavelet family carries a unique set of properties. For instance, Symlet wavelets are nearly symmetrical functions and Haar wavelets resemble a step function. *Figure 11* displays wavelet fingerprints taken from a TSOP IC using a "dmey" filtering wavelet and a "db3" wavelet transform. The plots were generated by taking 48 waveforms from different location on the IC and applying the wavelet fingerprinting algorithm at each point. The wavelets used in the transform can be changed as is demonstrated by *Figure 12*. *Figure 12* displays data taken from the same chip as in *Figure 11* with a "haar" filtering wavelet and a "mexh" wavelet transform applied. Changing the wavelets brings out different features of the data that may be more easily identified by the human eye. Features, such as a different number of rings, or a missing print, would be useful in differentiated a controlled chip from a flawed chip. *Figure 13* displays wavelet fingerprints taken from a PLCC IC using a "dmey" filtering wavelet and a "db3" wavelet

transform. We examined wavelet fingerprints from both types of IC's including flawed and unflawed samples of each type. After systematic signal processing we determined that the 100MHz transducer does not propagate far enough into an IC to capture data from the back face where the flaws seem to be located.

RESULTS FROM 50MHZ TRANSDUCER

We then purchased transducers of lower frequency (30, 50 and 75MHz). Lower frequency transducers are less sensitive to smaller flaws but penetrate deeper into a sample due to the lower attenuation. The stabilizer arm was constructed in such a way as to allow transducers to be swapped with ease. We began collecting data with the 50MHz transducer of both control and flawed chips and applied the wavelet transform. We located a repeatable pattern in the wavelet fingerprints differentiating the chips with delamination flaws from the control chips. *Figure 15* highlights this difference [20].

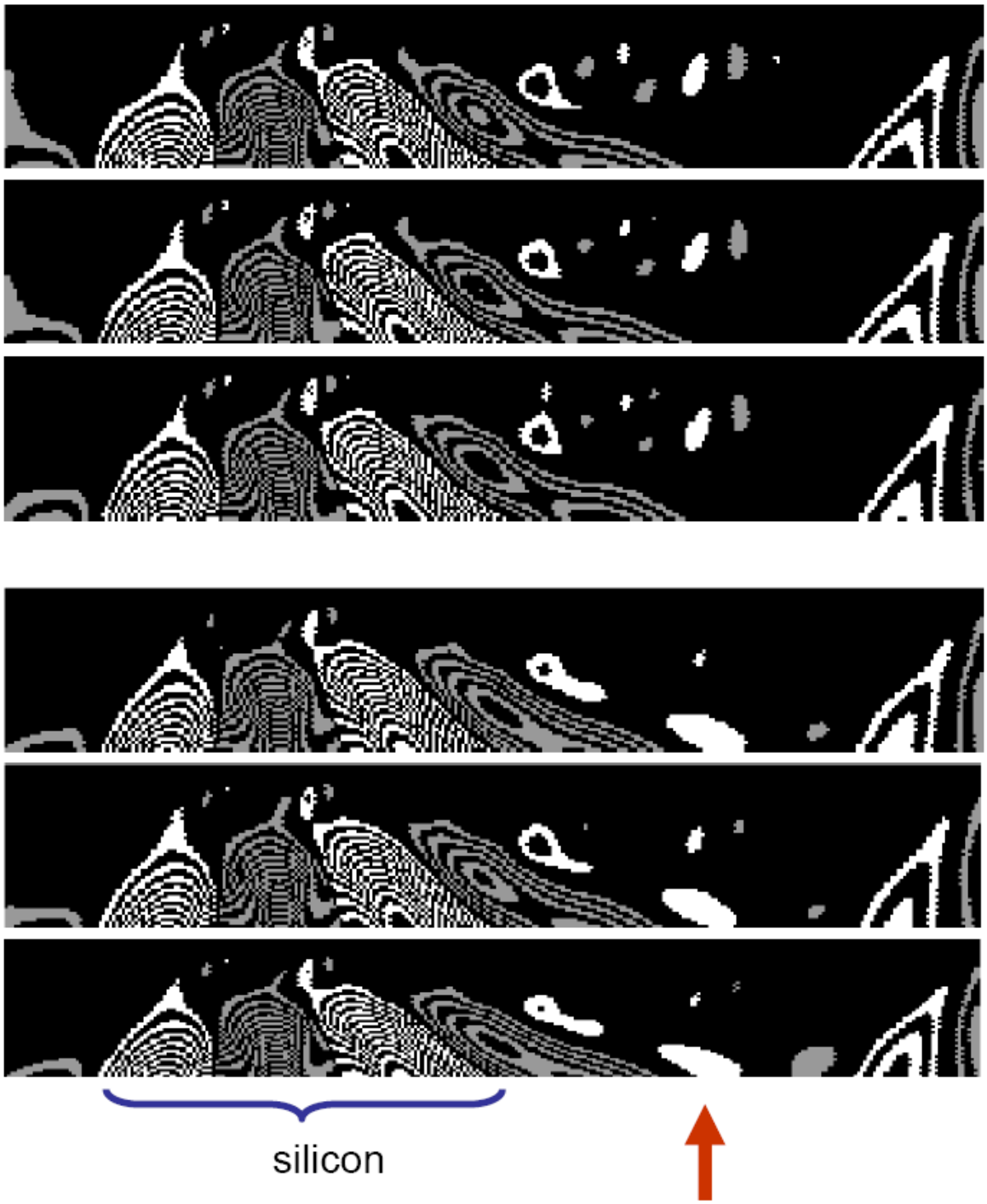


Figure 15: Shows wavelet fingerprints from three different flawed chips (top) and three different control chips (bottom) using a 50MHz transducer. Note the absence of the white oval (noted by the red arrow) in the flawed chips. This denotes the presence of a delamination flaw.

The three wavelet fingerprints from flawed chips displayed at the top of *Figure 15* lack a white oval found consistently in the in the control chips shown at the bottom of the figure [20]. *Figure 16* displays data taken from a control chip in the approximate grid over the entire surface of the chip [20]. Note the consistent presence of the white oval. *Figure 17* displays data taken from a flawed chip [20]. Note the absence of the white oval over areas of the chip. This is where the delamination is located.

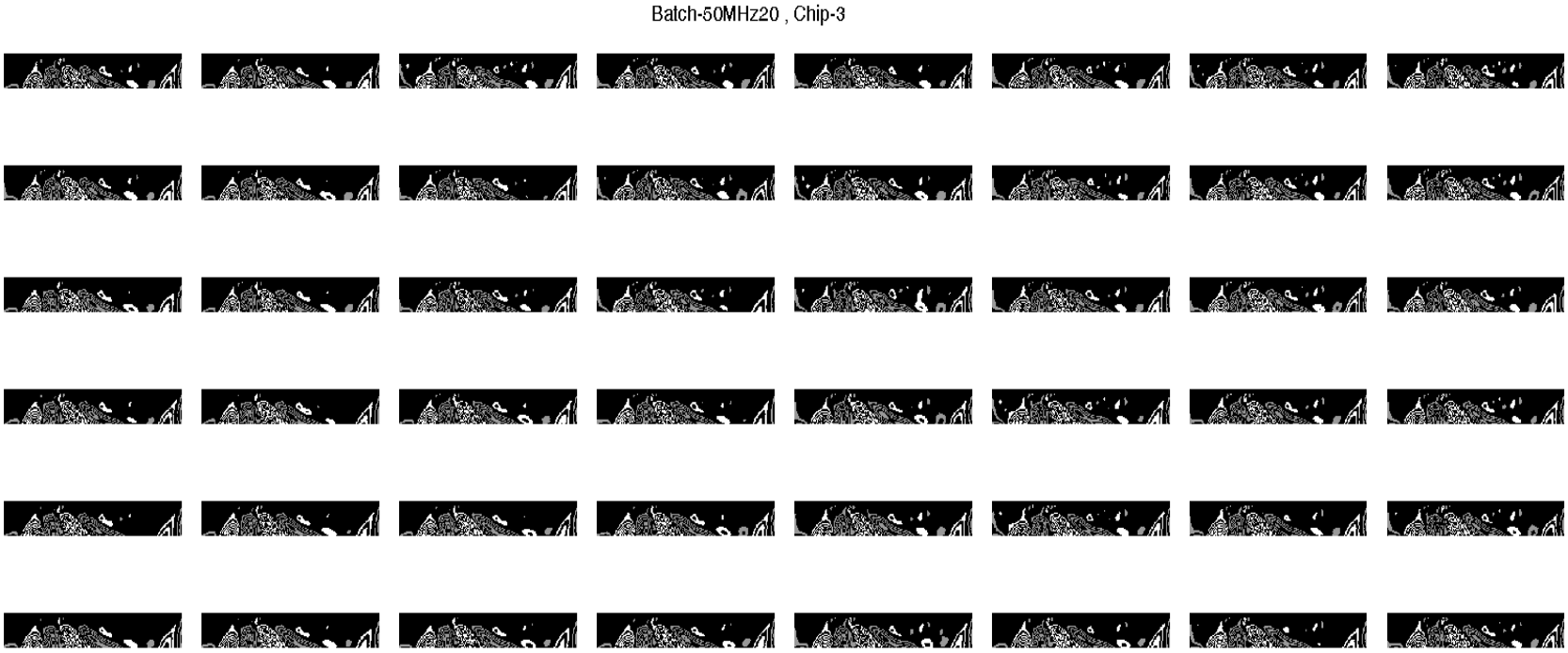


Figure 16: Wavelet fingerprints from a control chip using a 50MHz transducer. Note the consistent presence of the white oval throughout the fingerprints.

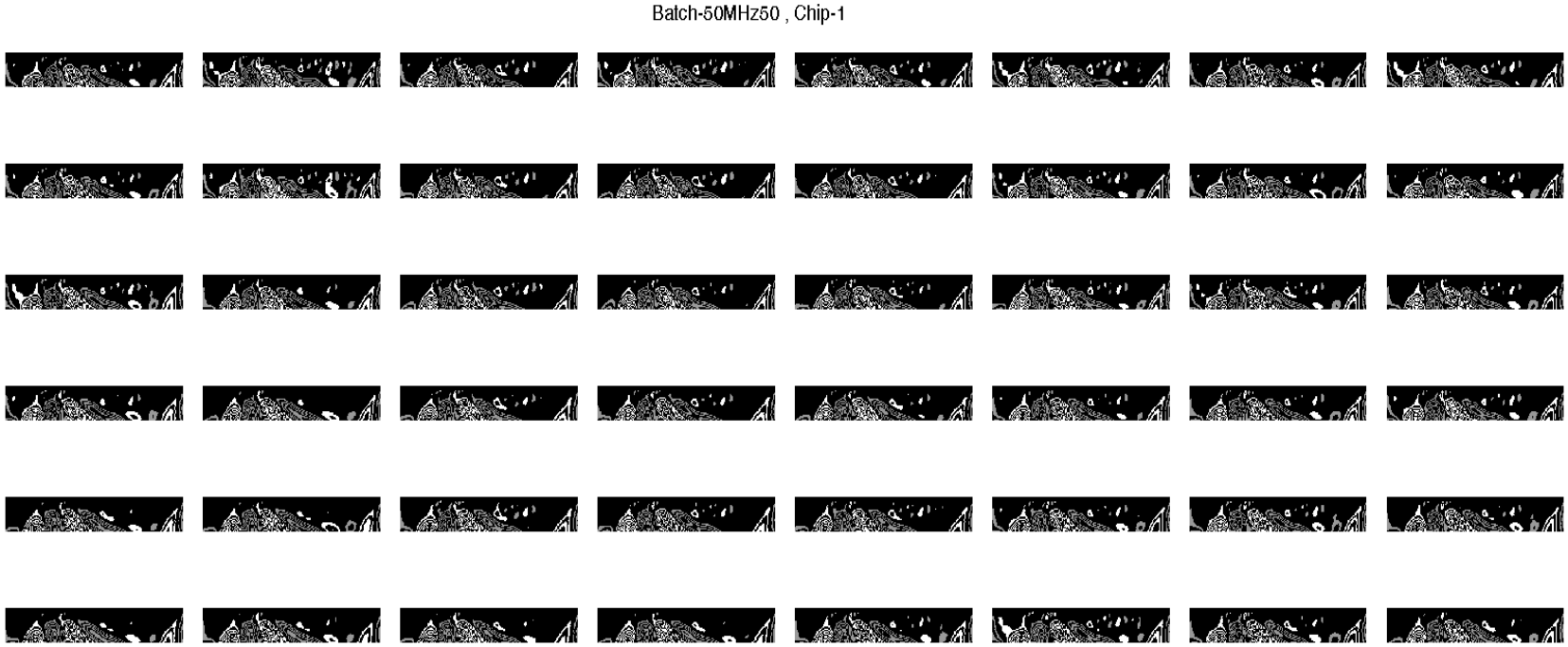


Figure 17: Wavelet fingerprints from a flawed chip using a 50MHz transducer. Note both the presence and absence of the white oval. The areas lacking the oval signify the delamination flaw.

The data confirms the success of this part of our research. We introduced delamination flaws into ICs and were able to detect them using a portable, inexpensive, non-destructive, high frequency, ultrasound test. We developed a program that automates the detection of the white oval in the fingerprints eliminating the need for visual detection and increasing the ease of use. This program returns a "1" for a fingerprint lacking the white oval (delaminated) and a "0" for a print with the white oval (free of delamination) as shown by *Figure 18*. *Figure 18* displays a flawed chip.

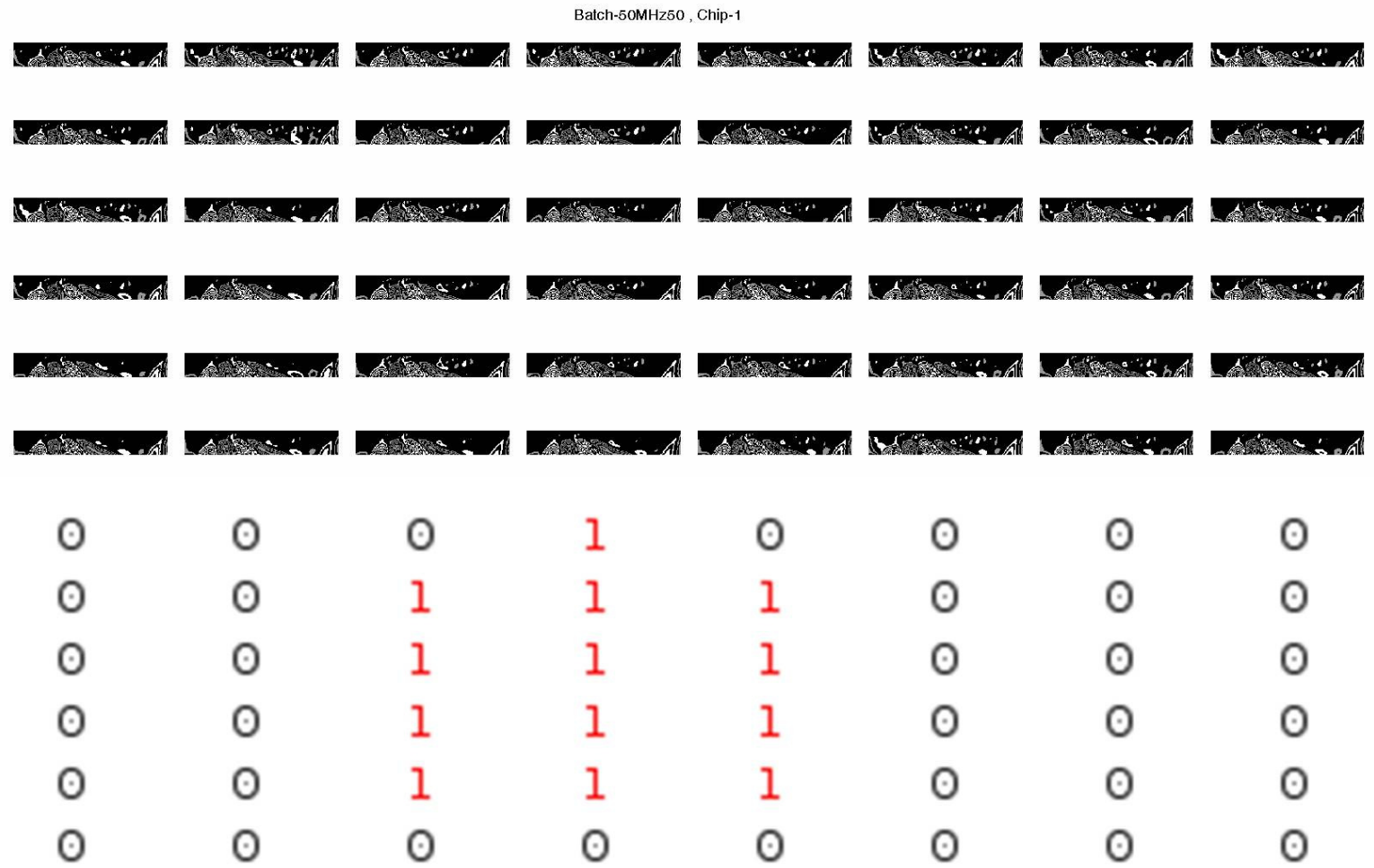


Figure 18: Demonstrates the automated method of detecting the presence or absence of a delamination flaw within a given wavelet fingerprint. Each print above corresponds to either a "1" (flawed) or "0" (not flawed) below.

The next step was to confirm our results by using an alternate means of detecting delamination flaws in microelectronics.

BACKGROUND FOR CONFIRMING RESULTS

Immersion testing is a common means of ultrasonic testing whereby a specimen is submerged in water, the transducer is fixed above it, and the water acts as the coupling agent. The transducer sends and receive ultrasonic pulses and a computer records waveforms (A-scans, *Figure 3)*, just as was done using our developed handheld device. Immersion testing is convenient because the scanning process can be automated and computer controlled, allowing for exact grids of data to be taken over a specimen. This enables imaging.

B-scan and C-scan plots are two types of images that can be generated using immersion testing. *Figure 19* demonstrates how both B and C-scans are formed [23].

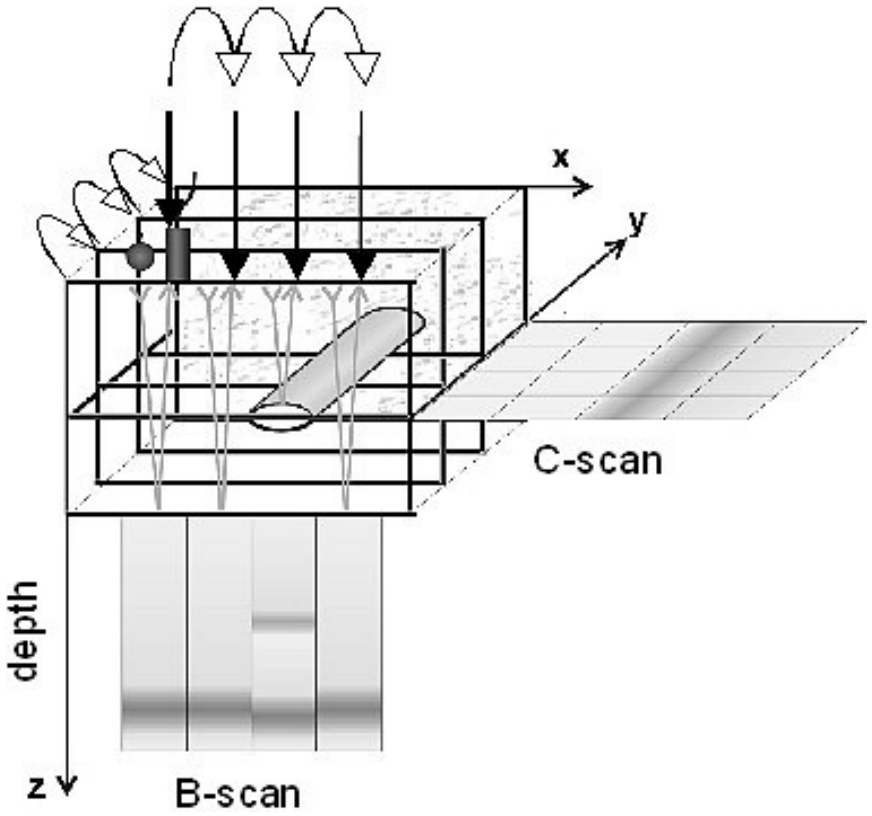


Figure 19: Demonstrates the process of forming B and C-scans. B-scans are formed by taking data in a cross-sectional slice across a single axis over the sample. C-scans are formed by taking data across two axes over the entire sample and displaying a plan-view version of the data [23].

Pulses are sent down upon the sample by a transducer and the waveforms are recorded. B-scans are formed by collecting waveforms along a straight line (single axis) across a specimen. Data is plotted displaying the distance across the specimen versus sample number (depth into the sample) and the amplitude of the waveform at a particular depth is displayed by means of color or shading. This is similar to a cross-section when making a cut perpendicular to the top face of the specimen. See *Figure 20* below.

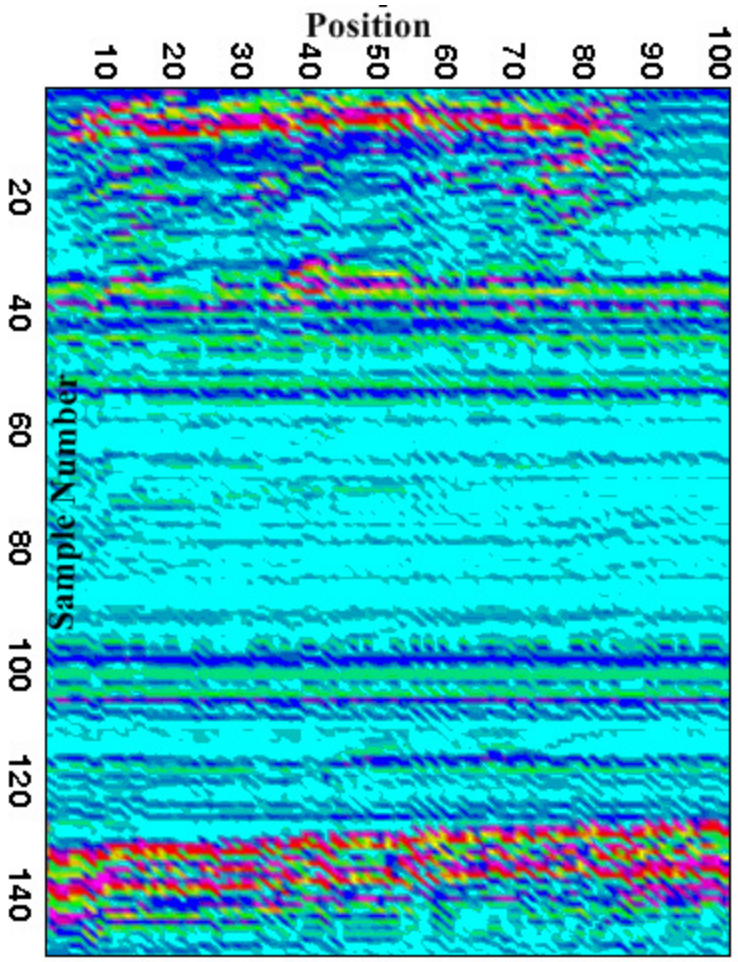


Figure 20: B-scan of an IC. Plot of sample number vs. distance across a specimen. The colors display the amplitude at a particular depth in the sample. The bright colored collection of lines at the top of the plot represent the top face of the IC and the bright colored collection of lines near the bottom represent the surface the chip was resting on.

This plot displays a B-scan of an IC. The bright colored collection of lines at the top of the plot represents the top face of the IC and the bright colored collection of lines near the bottom represents the surface the chip was resting on.

C-scans are formed by collecting waveforms in a grid like fashion (two axes) over a specimen. Data is plotted on an x-y grid, corresponding to position, and the colors refer to the amplitude of the waveform at a gated depth. The depth, or sample number, must be gated around values before the plot is generated. This is similar to viewing the floor

plans of a multi-story building. Each level of the building has different features that are discerned by viewing a single story's floor plan. See *Figure 21* below.

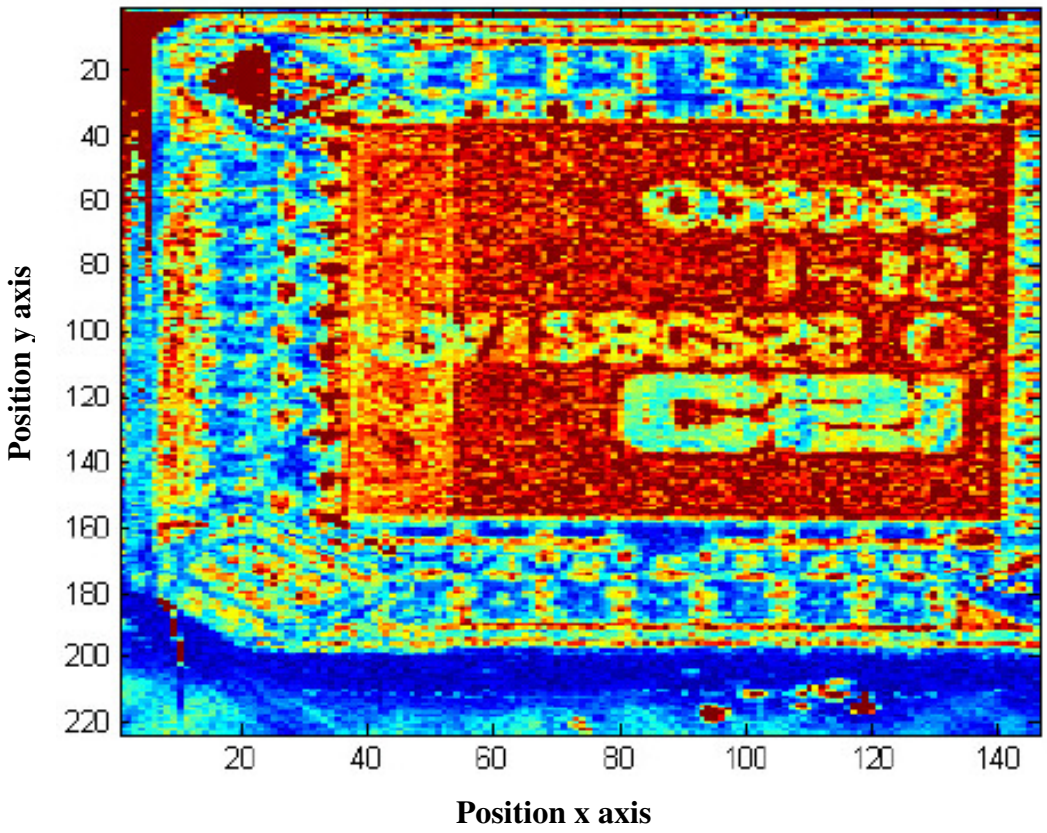


Figure 21: C-scan of an IC gated around the surface of the chip. The x and y axes display position, with the colors representing the amplitude of the reflection at the gated depth. This is similar to viewing a single story's floor plan of a multi-story structure.

B-scans and C-scans are useful tools because features of a sample are easily discerned by the untrained eye. The entirety of a sample can be viewed by displaying multiple scans back to back in quick succession (like a movie). For instance, after data is collected over a sample, a B-scan can be generated at the initial position displaying a cross section at, say, y = 1. In quick succession, B-scans are generated at y = 2, y = 3… etc. until the whole sample has been imaged. The same procedure can be applied to a C-scan except instead of changing the position of the cross section, the gated depth is changed so as to

view an image of the sample at varying depths below the surface of the top face of the sample.

PLAN FOR CONFIRMING RESULTS

We scanned both control and flawed chips in an immersion tank: *Figure 22*. We focused on the thin TSOP IC because we are confident of the presence of delaminations and were able to detect them using our portable device.

Figure 22: Ultrasonic immersion tank used to scan flawed and control chips for confirming our results. The process is automated and computer controlled.

The tank-scan apparatus automates the movement of the transducer over a chip, which has been submerged, and records waveforms in a grid. The number of waveforms recorded must be specified and will affect the resolution of the images. The waveforms are saved to a PC where we used a program we developed to compile B-scan and C-scan

images from the waveforms. Here is a graphical user interface that we wrote in Matlab to image and save A, B, and C-scan, *Figure 23*.

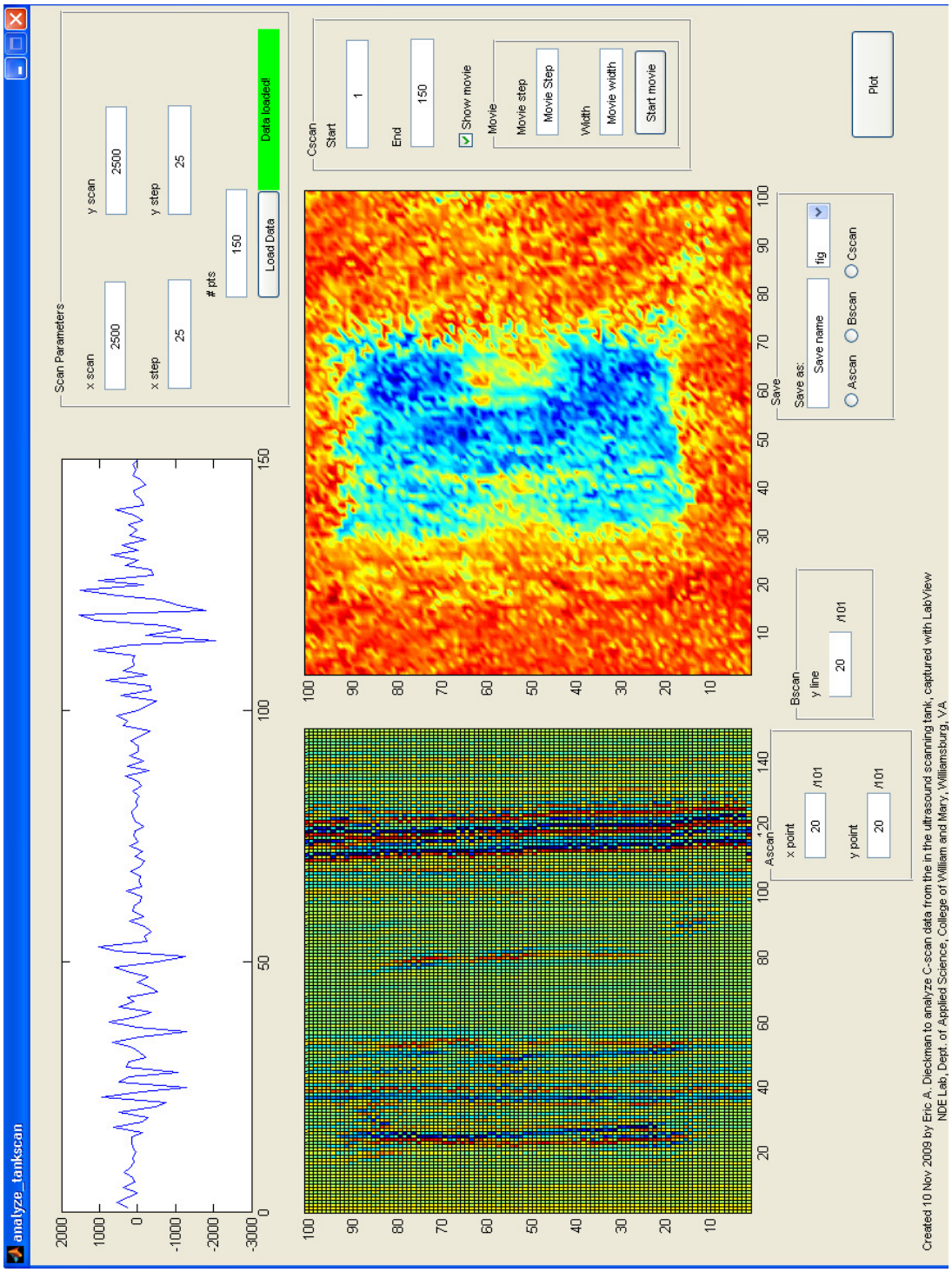


Figure 23: Tank-scan graphical user interface we have developed to image and save A,B, and C-scans. The parameters can be modified to permit data of different sizes. The location of A and B-scans can be specified as well as the gated depth of the C-scan. The GUI is also equipped with a C-scan movie option.

This GUI allows parameters to be modified to permit images of different spatial resolution. The coordinate of the A-scan can be specified as well as the line at which to view the B-scan along the y-axis. The gated depth of the C-scan can also be specified. The GUI is also equipped with a C-scan movie option where the number of data points to step through as well as the width of data points can be modified.

We began by sealing the flawed chips to ensure that no moisture would seep into the delamination when submerged in the immersion tank. If moisture were to fill the delamination, the flaw would be much harder to detect as the sound waves would propagate through the gap in the chip. The air pocket created by the delamination creates a strong reflection due to the impedance mismatch.

IMMERSION TESTING RESULTS

We immersion tested a number of known flawed and control TSOPs using transducers at 50, 30, and 20MHz. We determined the 50MHz transducer was not compatible with our computer's hardware, because the A/D board only supported up to an 80MHz sampling rate. It's necessary to have a sampling rate at least double the transducer's frequency in order to capture accurate data. Instead, we focused on the 30MHz transducer. We collected 10,000 data points (waveforms) over each chip in a grid fashion and imaged the chip using C, and B-scans. We used the C-scan movie option on the developed GUI to determine the depth of interesting features in the data. The following figures correspond to C-scans gated near the back face (where we expected to see delaminations) of an IC using the 30MHz transducers.

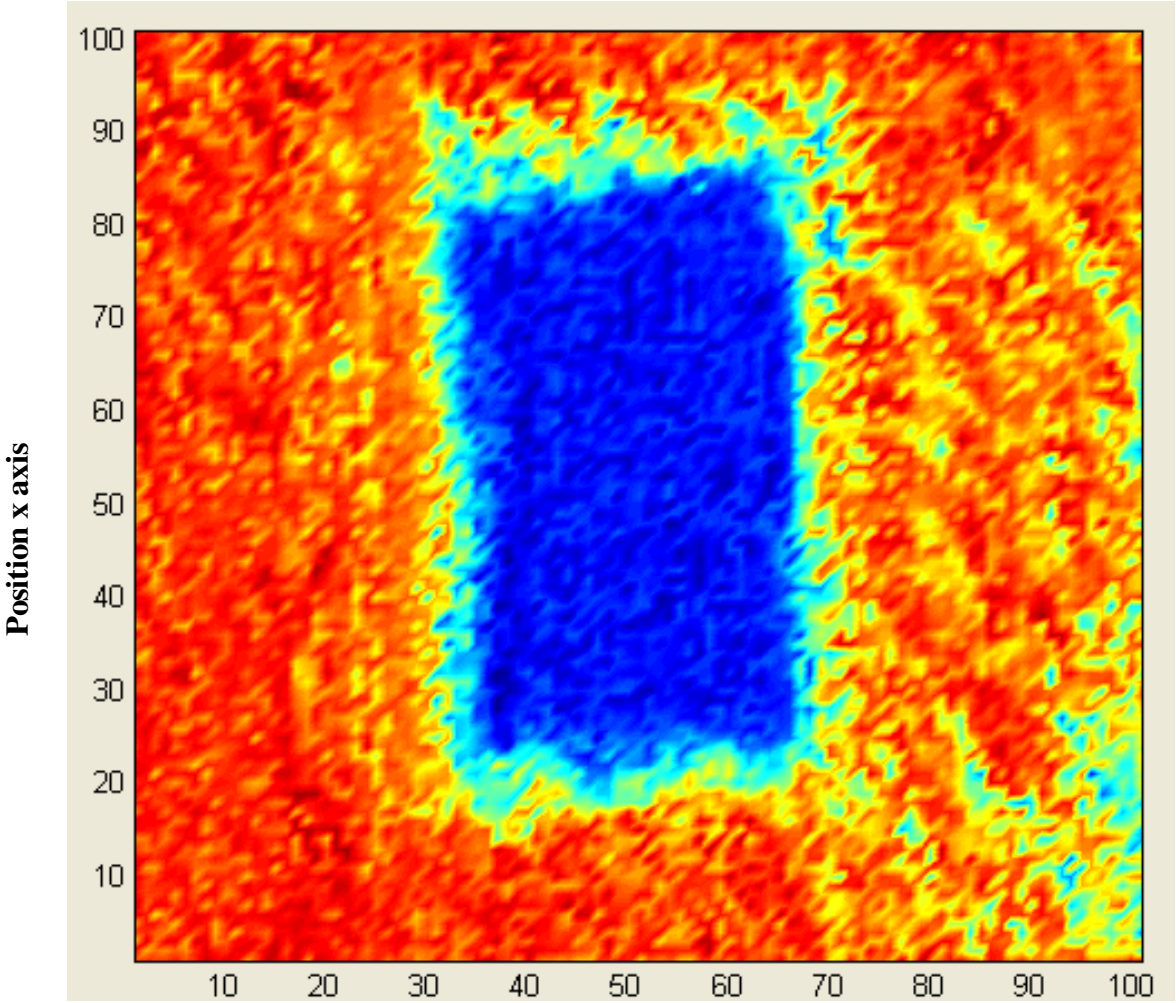


Figure 24: C-scan from control chip 20-3 using a 30MHz transducer. The dark blue rectangle corresponds to the chip scanned. No apparent delaminations were discovered within the chip.

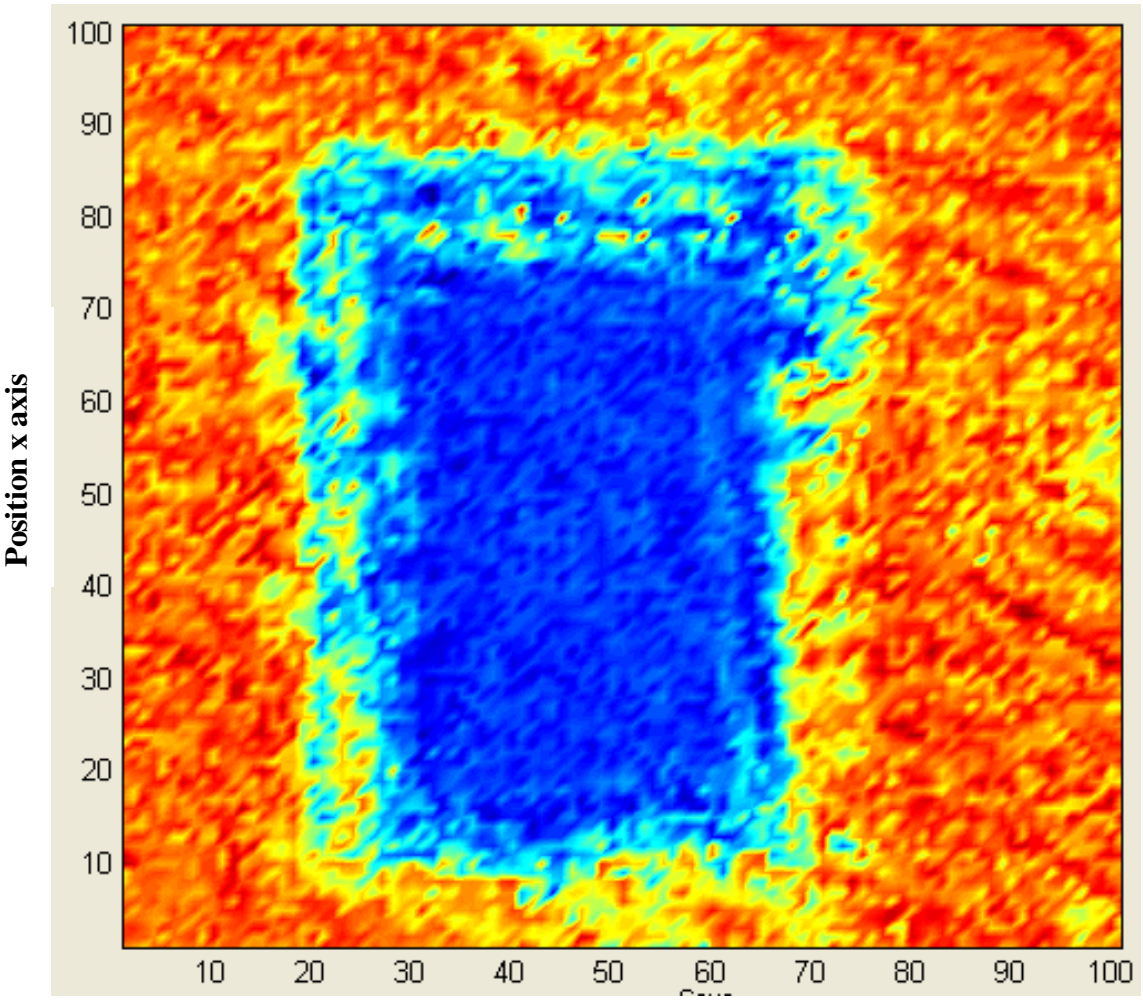


Figure 25: C-scan from flawed chip 50-1 using a 30MHz transducer. The dark blue rectangle corresponds to the chip scanned. No apparent delaminations were discovered within the chip.

After examining *Figure 24* and *Figure 25* we determined there to be no obvious difference between flawed and control chips. No apparent delaminations exist in the flawed chip: *Figure 25*. Further examination of the 30Mhz B-scans led us to believe that the 30MHz transducer was not propagating far enough under the surface of the chip to capture the interesting data near the back face of the chip. *Figure 26* displays an example of a B-scan of a chip using a 30MHz transducer.

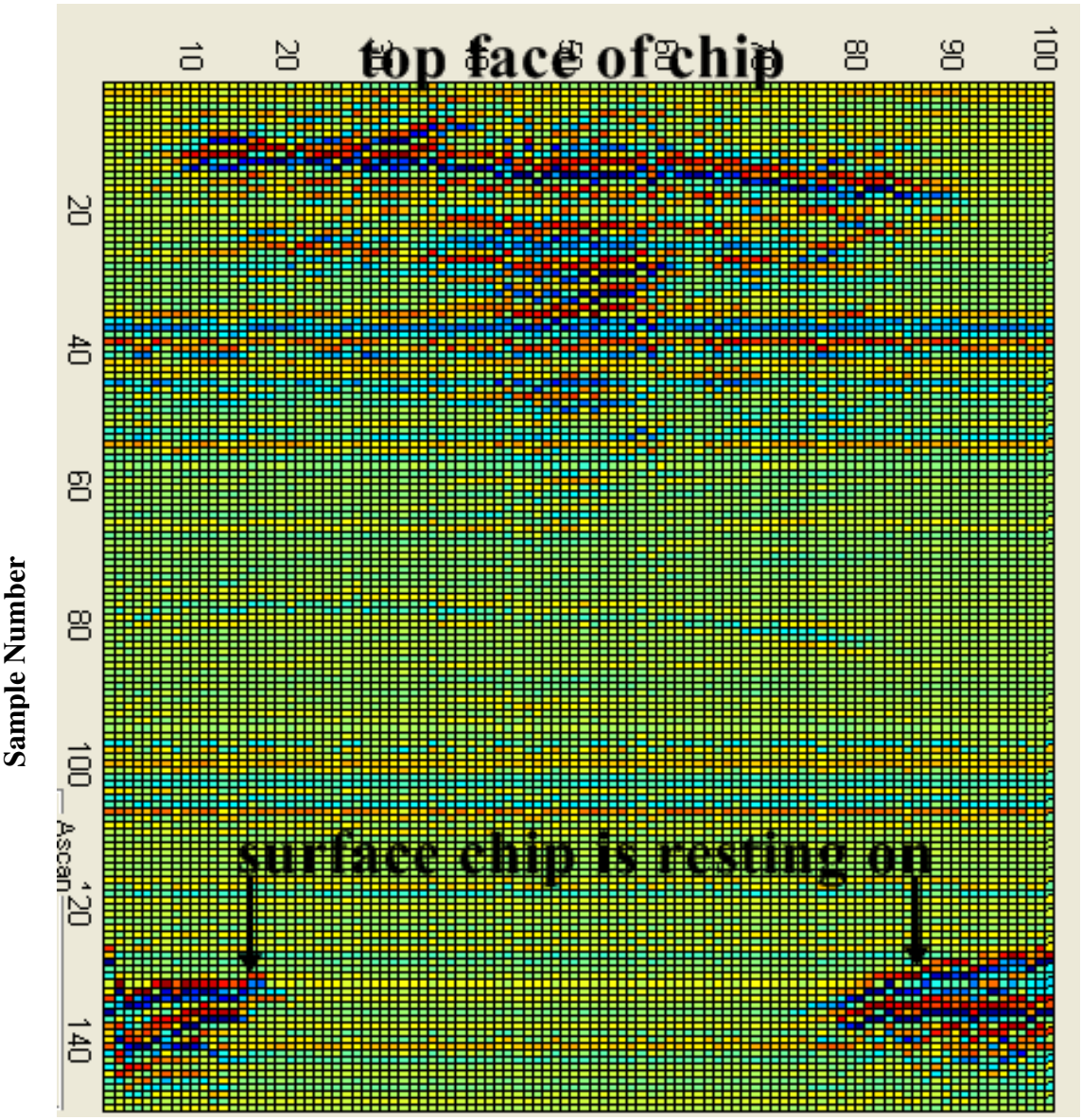


Figure 26: B-scan of a chip using the 30MHz transducer. Note the absence of reflections near the center and back face of the chip. It appears the ultrasonic pulses can only capture data approximately a third of the way through the chip and does not capture any data near the back face.

This B-scan illustrates the inability of the transducer to capture data deep into the chip. Reflections are only seen approximately a third of the way through the chip from the front face. There is a large absence of reflection from the center of the chip through the

back face. Then, we tested a chip using a 20MHz transducer which should propagate pulses deeper into the chip. The B-scans showed the 20MHz transducer was much better equipped to capture data deeper into the chip. *Figure 27* displays an example of a B-scan of a chip using a 20MHz transducer.

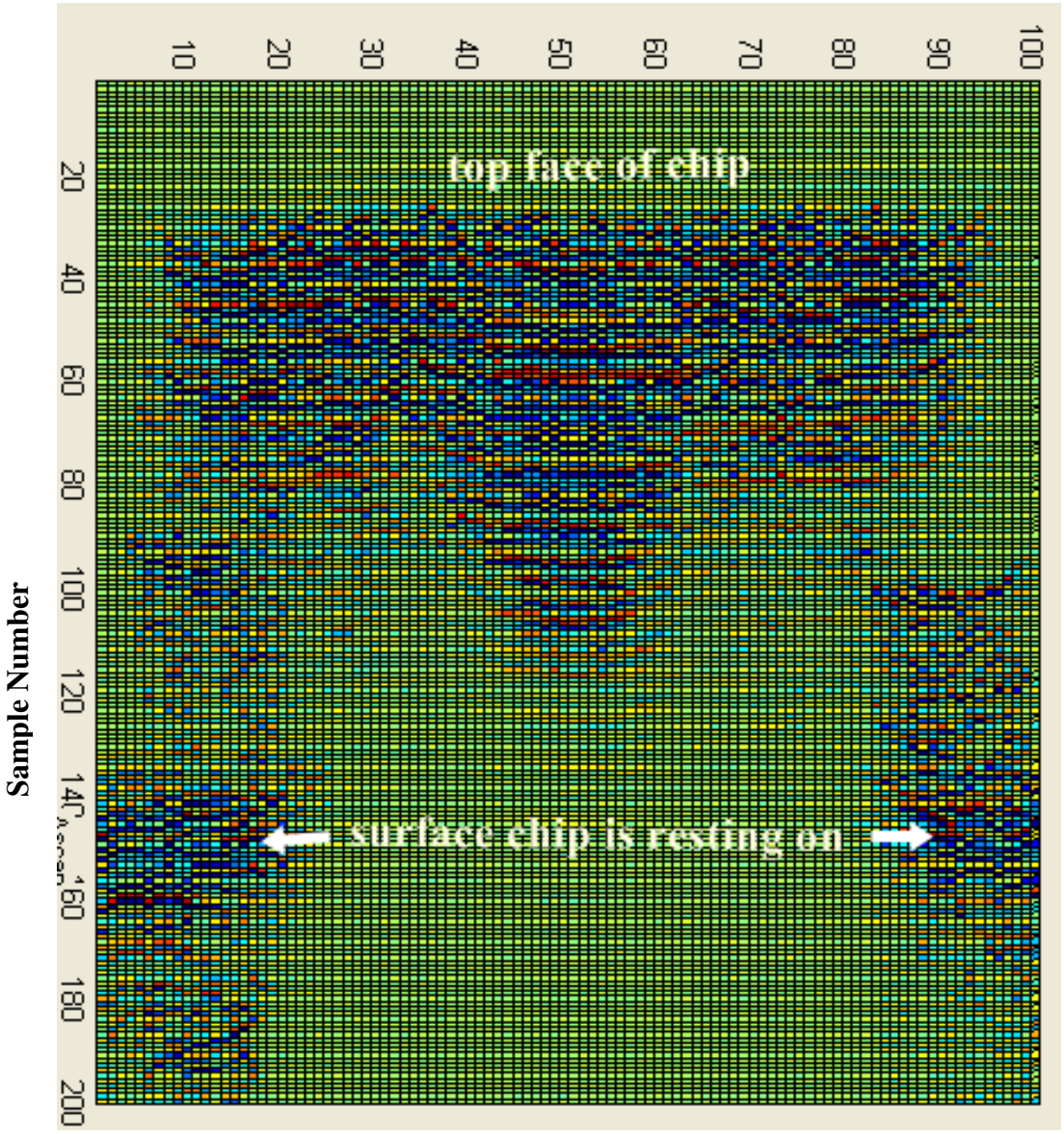


Figure 27: B-scan of a chip using a 20MHz transducer. Reflections can be seen much deeper into the chip than when using the 30MHz transducer.

In this case, the 20MHz transducer propagates pulses much further under the surface of the chip, and reflections can be seen closer to the back face where the delaminations likely occur.

At 20MHz, we saw strong reflections near the back face of the chip using C-scans. These reflection bursts correspond to the same delaminations detected using the portable device we developed. The following figures are examples of C-scans of both flawed and control chips gated near the back face of the chip. The first three C-scans correspond to flawed chips that we detected delaminations in the wavelets. The second two C-scans correspond to control chips neither subjected to the humidity chamber nor the reflow profile.

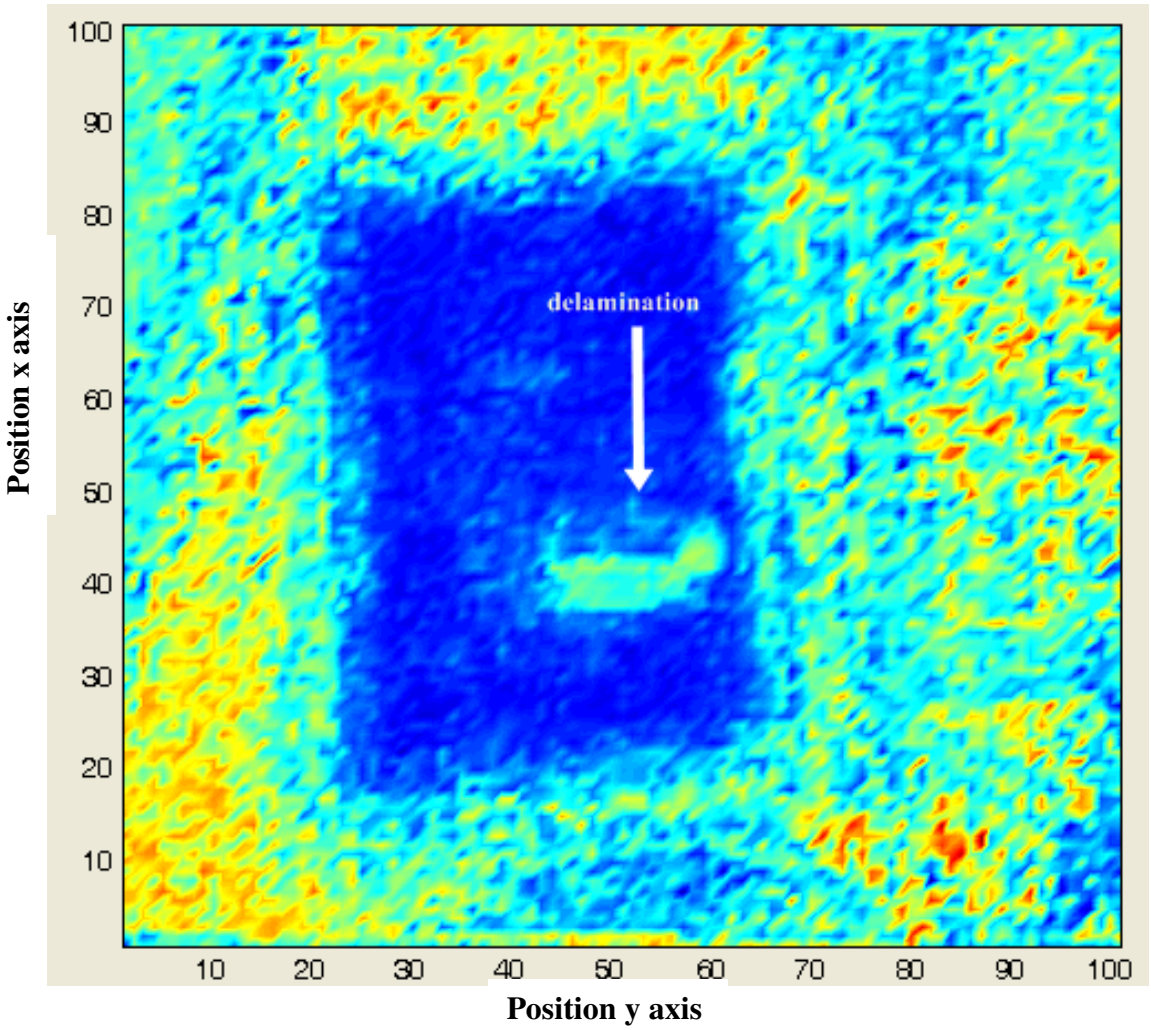


Figure 28: C-scan of flawed chip 40-3 gated near back face of chip. Note the light blue burst located within the rectangle (chip). This is a delamination.

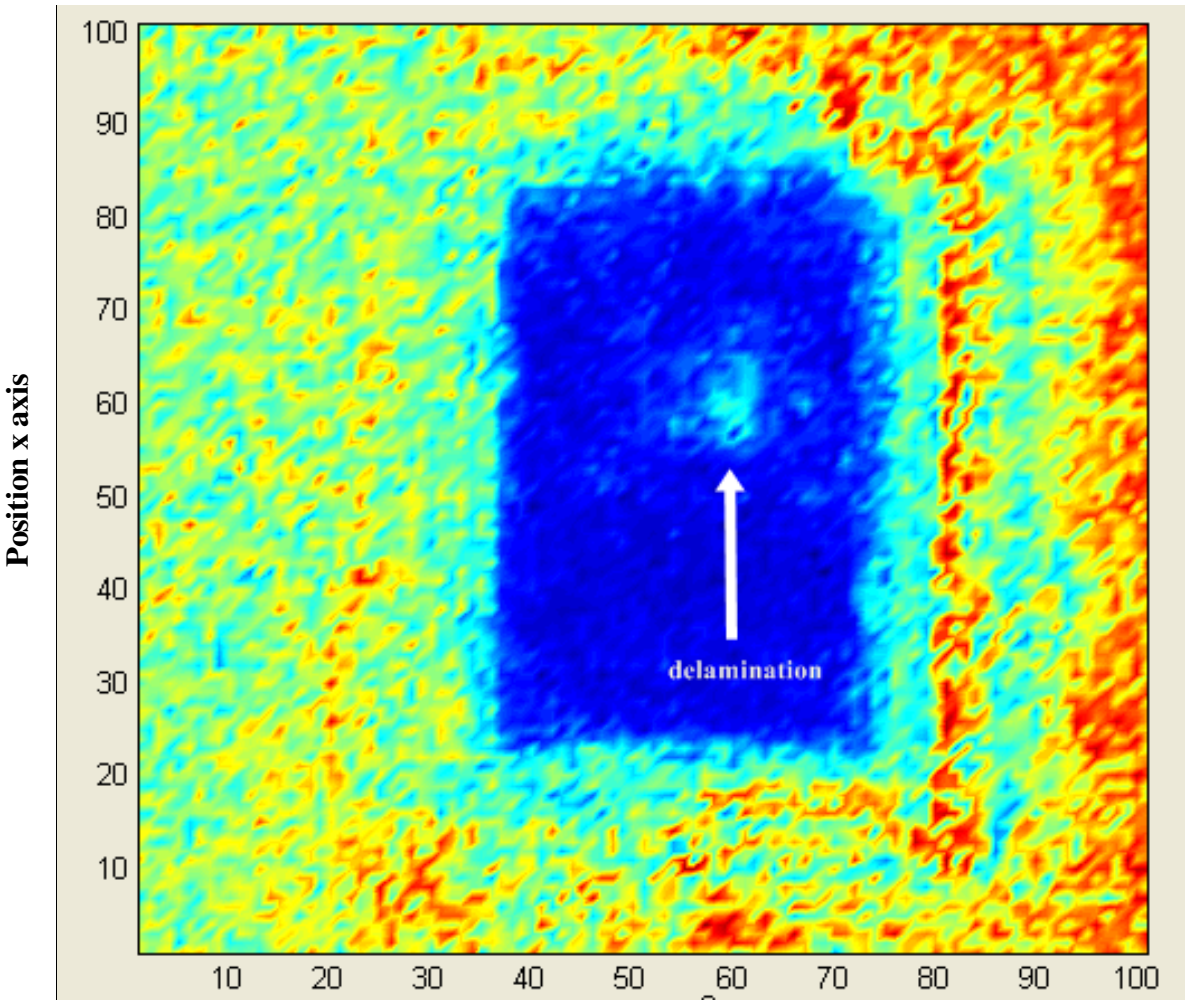


Figure 29: C-scan of flawed chip 50-1 gated near back face of chip. Note the light blue burst located within the rectangle (chip). This is a delamination.

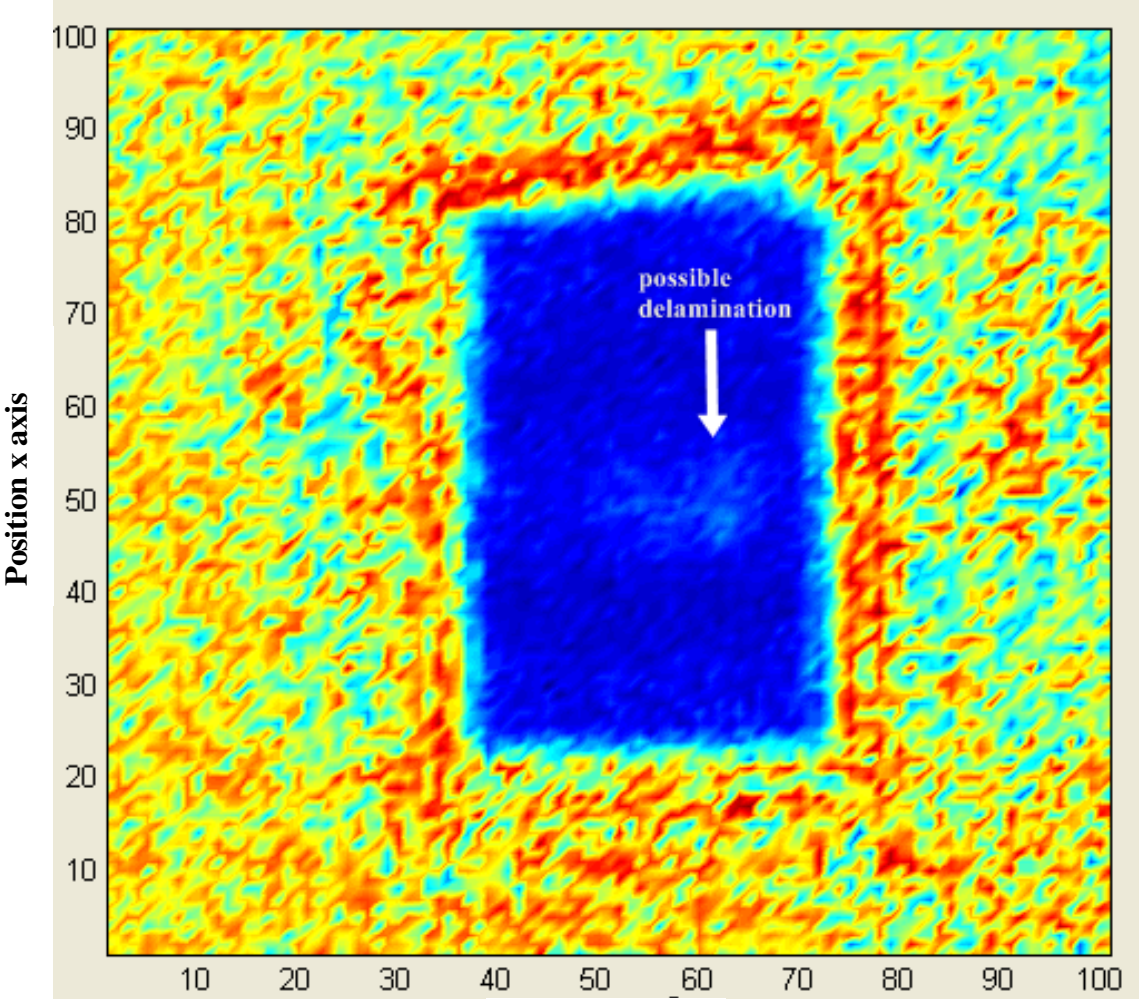


Figure 30: C-scan of flawed chip 50-3 gated near back face of chip. This chip shows possible signs of delamination in the C-scan; however, the reflection is not nearly as strong as in chip 40-3 and 50-1. The size of delamination must be smaller, thus harder to see.

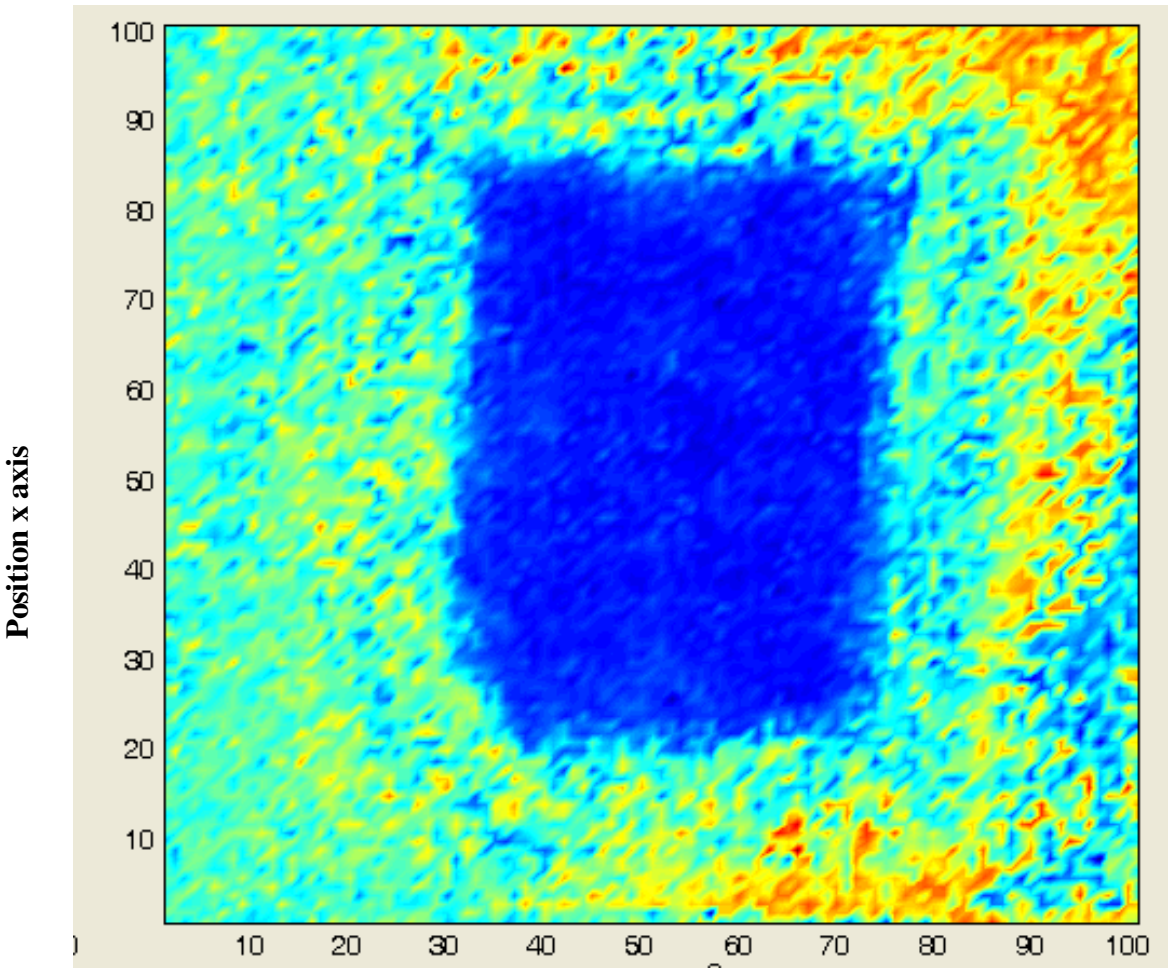


Figure 31: C-scan of control chip 20-2 gated near back face of chip. Note the absence of any signs of delamination

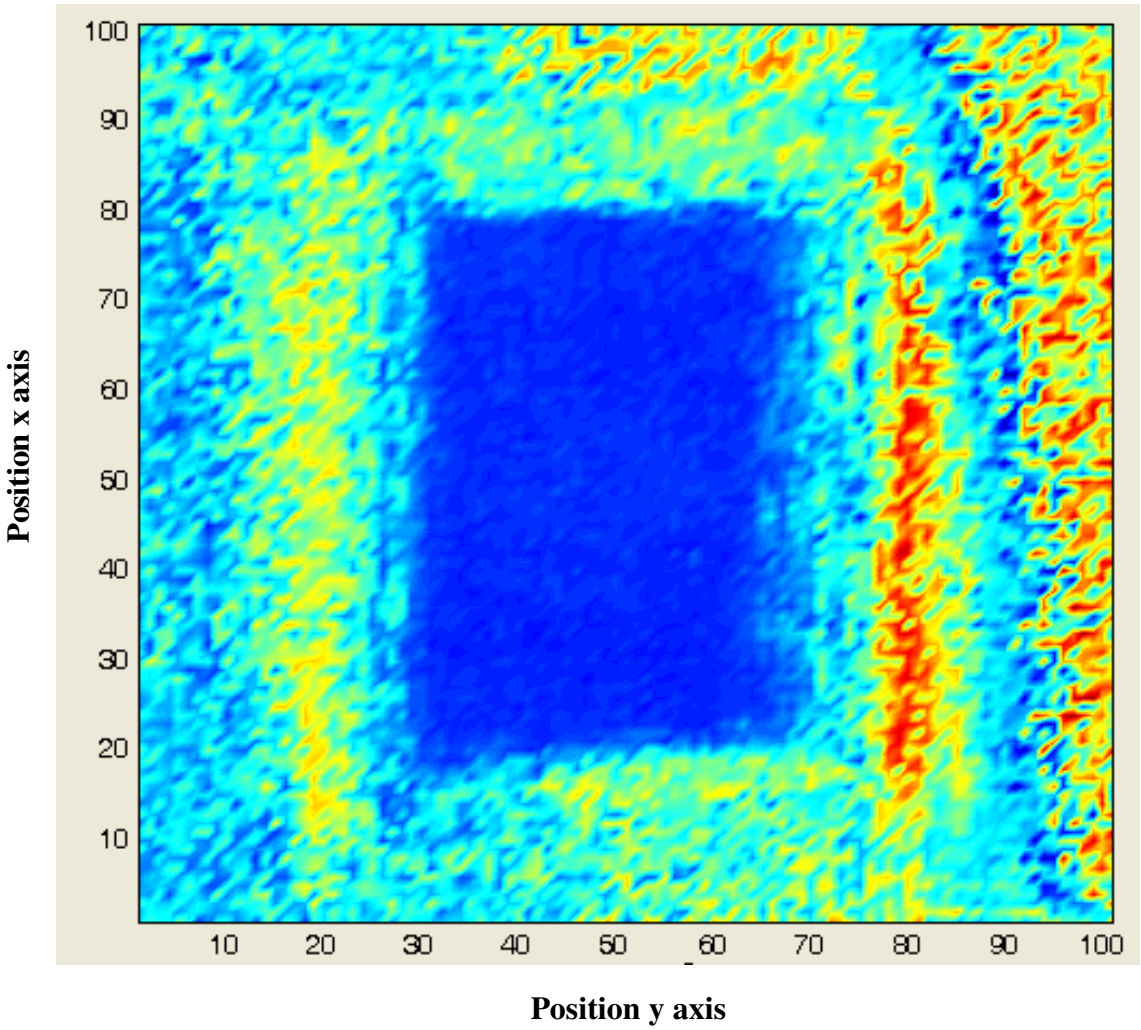


Figure 32: C-scan of control chip 20-3 gated near back face of chip. Note the absence of any signs of delamination

In *Figure 28* and *Figure 29* delaminations are clearly present, demonstrated by the light blue burst within the confines of the larger dark blue rectangle (chip). This is a reflection due to the gap between layers of the chip. The delamination is not seen in the two control chips, *Figure 31* and *Figure 32*. The dark blue area is free of any large reflections. And *Figure 30* is more difficult to decipher because the C-scan shows possible signs of delamination; however, the reflection is not nearly as strong as in *Figure 28* and *Figure 29*. It's likely the delamination is smaller in this chip.

After analyzing the tankscan data, we compared it to the results acquired from using the portable device and wavelet fingerprinting. We used the process that automates the flaw detection in the wavelet fingerprint data and compared it to the C-scans. *Figure 33* demonstrates how both processes show a chip is delaminated.

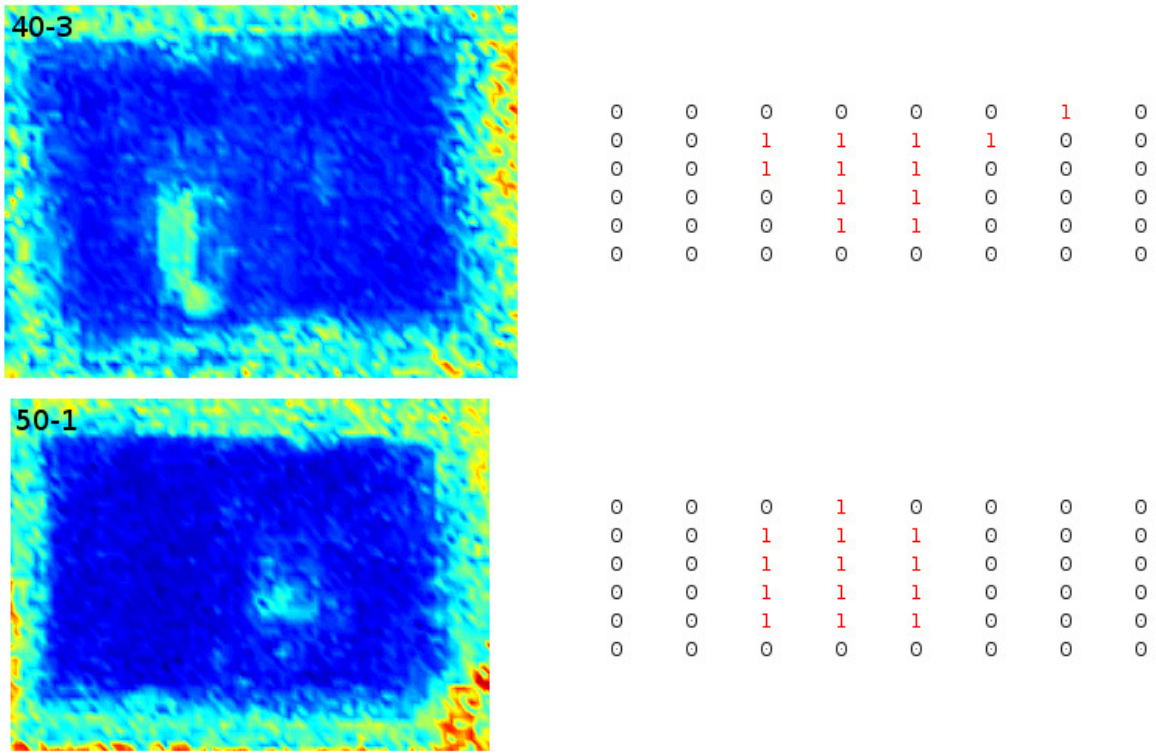


Figure 33: Displays how both the portable wavelet fingerprinting method and immersion testing can detect delamination flaws in chips. The C-scans on the left correspond to the same chip that the automated process pictures on right. The "1"s correspond to wavelets showing delaminations and the "0"s correspond to wavelets lacking delamination features.

The C-scans pictured left correspond to data taken from the same chip as the automated process at right. The presence of the light blue reflection burst in the C-scan, and the presence of an area of "1"s confirms that both the C-scan and the automated methods demonstrate the presence of flaws.

CONCLUSION

We have developed a portable, high-frequency, contact, ultrasonic apparatus for detecting delamination flaws in integrated circuits through the construction of a bench-top apparatus and the adaptation of the Dynamic Wavelet Fingerprint technique. The developed technology has the capability of detecting smaller flaws through an inexpensive, portable device, which has not been previously done. We demonstrated success in introducing and detecting delaminations in the thin TSOP ICs, as confirmed through immersion testing. Further research must be conducted with respect to the nature of delamination in PLCC ICs.

REFERENCES

[1] Proceedings of the symposium on avoiding, detecting, and preventing counterfeit electronic parts, UMD CALCE, SMTA. Edina, MN. 2009

[2] Shapiro, Lev. "Counterfeit Electronics: Threats, Risks and Prevention Practices." EMS007. (2010)

[3] *SCRM for IT Electronics*, General Dynamics Advance Information Systems

[4] Adee, Sally. "Are chip makers building electronic trapdoors in military hardware? The Pentagon is making its biggest effort yet to find out." IEEE. (2008).

[5] *High-Frequency Contact Ultrasound for Subsurface Characterization of Microelectronics,* (M. Hinders, E. Dieckman and J. Stevens) ASNT 19th Annual Research Symposium, Williamsburg, VA, 22 March 2010.)

[6] Bray, Don, and Roderic Stanely. *Nondestructive Evaluation*. Rev. ed. Boca Raton, FL: CRC Press, 1997.

[7] J. Hou and M. Hinders Dynamic Wavelet Fingerprint Identification of Ultrasound Signals Materials Evaluation 60, #9 1089, (2002).

[8] J. Hou, M. Hinders and S.T. Rose) Ultrasonic Periodontal Probing

Based on the Dynamic Wavelet Fingerprint J. Applied Signal Processing, Vol. 2005, No. 7, 1137-1146 (2005).

[9] J. Hou, K. R. Leonard and M. Hinders, Automatic Multi-mode Lamb Wave Arrival Time Extraction for Improved Tomographic Reconstruction Inverse Problems 20, 1873-1888 (2004).

[10] K. R. Leonard and M. Hinders, Lamb wave tomography of pipe-like structures Ultrasonics, Vol. 44, #7, 574-583 (2005).

[11] K. R. Leonard and M. Hinders, Multi-mode Lamb Wave Tomography with Arrival Time Sorting JASA, Vol. 117, #4, 2028-2038 (2005).

[12] M. Hinders, J. Hou, J.C.P. McKeon, Wavelet Processing of High Frequency Ultrasound Echoes from Multilayers in "Reviews of Progress in Quantitative Nondestructive Evaluation Vol. 24", D.O. Thompson and D.E. Chimenti, eds. 1137-1144 (2005).

[13] M. Hinders, R. Jones and K. Leonard, Wavelet Thumbprint Analysis of Time Domain Reflectometry Signals for Wiring Flaw Detection Engineering Intelligent Systems vol 15, #4, 65-79 (2007).

[14] J. Bingham and M. Hinders, Lamb Wave Charactrization of Corrosion-Thinning in Aircraft Stringers: Experiment and 3D Simulation JASA, Vol 126, #1, 103-113 (2009).

[15] J. Bingham, M. Hinders and A. Friedman, Lamb Wave Detection of Limpet Mines on Ship Hulls Ultrasonics, in press (2009).

[16] C. Bertoncini and M. Hinders Binary Detection Algorithm for the Ultrasonographic Periodontal Probe Pattern Analysis and Applications, in press (2009).

[17] C. Bertoncini, M. Hinders and S. Ghoryeb Ultrasonographic detection of tooth flaws Review of Progress in Quantitative Nondestructive Evaluation, Vol. 29, to appear, AIP Press (2010).

[18] C. Bertoncini and M. Hinders Detection of Mine Roof-Fall Precursers in Microseismic Signals Review of Progress in Quantitative Nondestructive Evaluation, Vol. 29, to appear, AIP Press (2010).

[19] Matlab Help Toolbox. www.mathworks.com/products/wavelet

[20] M. Hinders, *Handheld High-Frequency Ultrasound Detection of Disbonds in Microchips*, final technical report for General Dynamics Advanced Information Systems, December 2009.

[21] Federal Highway Administration, Guidelines for Ultrasonic Inspection of Hanger Pins, http://www.tfhrc.gov/infrastructure/nde/pubs/04042/02.htm, July 2004

[22] National Instruments, Fundamentals of Ultrasonic Imaging and Flaw Detection, http://zone.ni.com/devzone/cda/tut/p/id/3368, February 2010

[23] C. Kohl, M. Krause, C. Maierhofer, J. Wostmann, H. Wiggenhauser, and K. Mayer, *3-D Visualization of NDT-Data using Data Fusion Technique*. International Symposium: Non-Destructive Testing in Civil Engineering 2003.