Development of a High-Speed Photography System

A thesis submitted in partial fulfillment of the requirement
for the degree of Bachelors of Science in Physics from
The College of William and Mary in Virginia.

by

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Introduction

Capturing fast events on film, such as the impact of water droplets, objects shattering, deformation of objects during collisions, and more, requires techniques and equipment beyond the realm of conventional photography. This project includes the development, construction, and implementation of a complete customized high-speed photography system.

In order to detect and image fast moving events, the high-speed photography apparatus must include four major components: a triggering mechanism, a delay controller, a high-speed flash, and a camera. These components communicate with one another to detect a moving object, implement a preset delay, and take a photograph that is exposed by a 10^{-5}s duration flash. The overall goal of this project is to observe and capture events too rapid to be seen with the naked eye in a manner that is both artistically pleasing and scientifically important.

History

In the 1950's, MIT electrical engineer Harold Edgerton pioneered the field of high-speed photography. Combining photographic artistry with technical mastery, he uncovered a bizarre and beautiful world of fast moving objects, frozen in time on an unprecedented level. His classic images include the "Milkdrop Coronet" and "Shooting the Apple," as shown in Figure 1.

Edgerton recognized the principle components needed for a successful high-speed photography system: short-duration flashes, reliable triggers, and controllable delays.[1] In the pre-semiconductor era, he began development with vacuum tubes and early xenon lamps. He was highly successive in his work and has a museum in his honor at MIT.

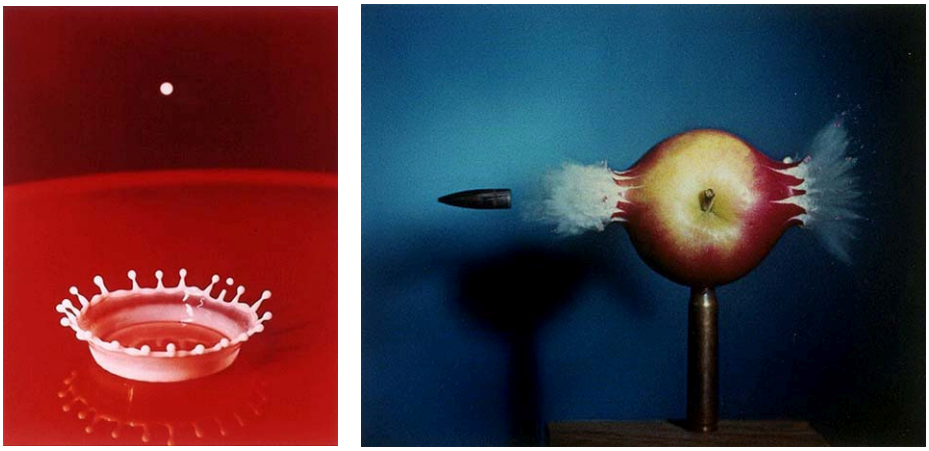

Figure 1 Edgerton's "Milkdrop Coronet"[2] and "Shooting the Apple"[3]

A modern day inspiration for the development of a customized high-speed photography system comes from Martin Waugh, a physicist and photographer based out of Portland, Oregon. Waugh has studied and perfected the high-speed photography of liquids in motion. By controlling color, lighting, viscosity, velocity, and timing of fluid drops, he is able to exercise a great deal of control over the image, as seen in the samples of his work below (Figure 2). His gallery is available online.[4]

Figure 2 Waugh's "Blue Staff"[5] and "Touch of Cream 2"[6]

Overview of the High-speed Photography System

The high-speed photographic system developed in this project consists of four major parts: the trigger, the delay controller, the flashes, and the camera, as shown in Figure 3. In the block diagram, the high-speed system is configured to capture the impact of a water droplet on a surface, pictured in Figure 4.

The first component in the system, the trigger, is a sensor designed to detect the moving object that will create the event. An infrared photogate trigger detects the falling droplet when it breaks the infrared beam and signals the delay controller with an electric pulse. The delay controller counts down a precise delay, controllable from microseconds to milliseconds, before signaling the camera to take a picture and firing the flashes. In this example, the delay controller counts down the exact amount of time it takes for the water droplet to fall from the photogate to the surface where it will impact. This delay is programmable. When the countdown of the delay controller reaches zero, it signals the flashes to fire. By the nature of their ultra-short duration, the flashes enable the freeze-frame illumination of very fast events.

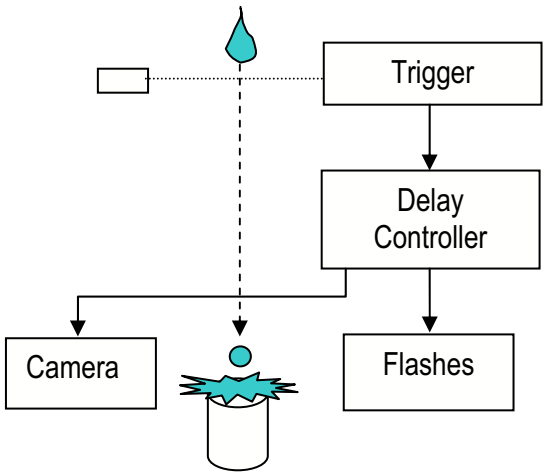

Figure 3 High-speed photography system block diagram, showing how a falling water droplet activates an event trigger, which communicates with the delay controller, which then communicates with the camera and high-speed flashes.

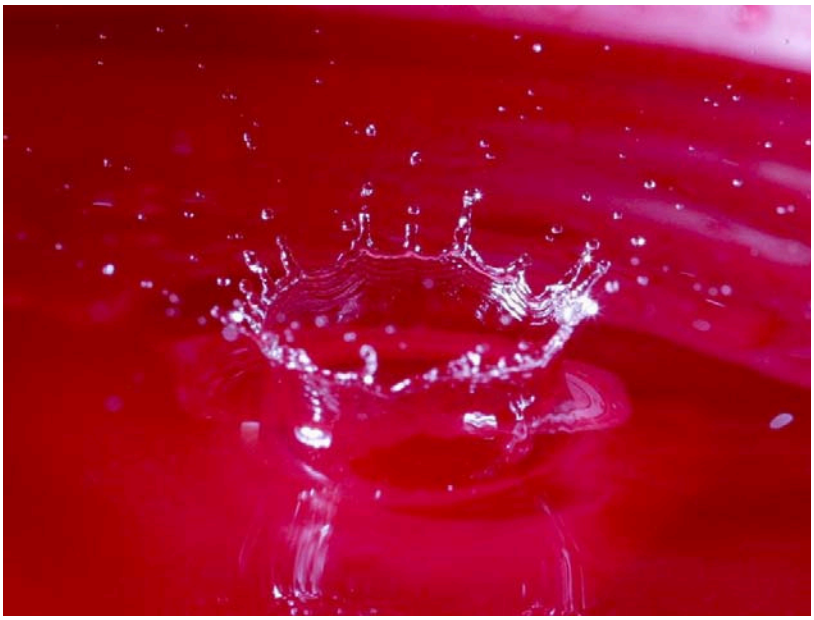

Figure 4 Crown shape, captured just milliseconds after water droplet impact on red plastic

Triggers

The purpose of the triggers is to detect an event and signal the delay controller. An infrared photogate trigger has been designed and built. The photogate trigger detects an event when an object passes between an infrared (IR) light emitting diode (LED) and an infrared phototransistor, thereby partially (or completely) obstructing the infrared beam.

Figure 5 illustrates the schematic for the infrared photogate trigger. Note that the IR LED is positioned so that its radiation is incident on the phototransistor, as seen in Figure 6. Sensitivity to partial or full beam obstruction is determined by adjusting R1, a 5kΩ 20-turn precision potentiometer that serves to current limit the infrared LED, and thus set the intensity of the beam. When the beam is disrupted, the NPN phototransistor's conduction is reduced, and the pull-down resistor R2 connected to the emitter of the phototransistor causes the potential to drop on the trigger input (pin 2) of the 555 timer IC, operated in one-shot mode. One-shot mode means that for

every trigger signal the chip detects, it responds with a single output pulse. When the voltage on the 555 trigger input drops below threshold (33.3% of the IC's supply voltage) the timer is activated and produces a positive logic pulse on the output, pin 3.

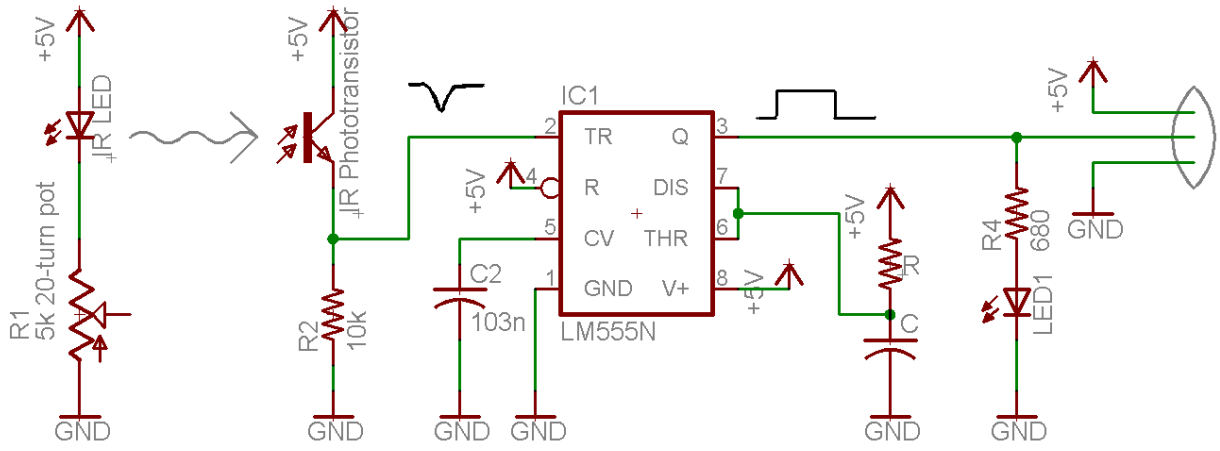

Figure 5 Infrared photogate trigger schematic diagram, with output cable shown at far right

The length of the pulse that the trigger circuit produces in response to an interruption of the infrared beam is determined by the rate at which capacitor C charges, which is determined by the series resistance-capacitance (RC) time constant formula in Equation 1:

$$\tau = RC \tag{1}$$

Due to the design of the 555 timer IC, it samples at a slightly higher voltage level, which corresponds to a response time of 1.1τ[7]. This is the duration of the output pulse. In the photogate trigger design for this project, the output pulse length was chosen to be approximately 0.1 seconds. The total length of the pulse duration is not critical because only the rising edge of the pulse (which occurs between 200ns and 1000ns after the infrared beam is interrupted) is used to communicate with the next component in the system, the delay controller.

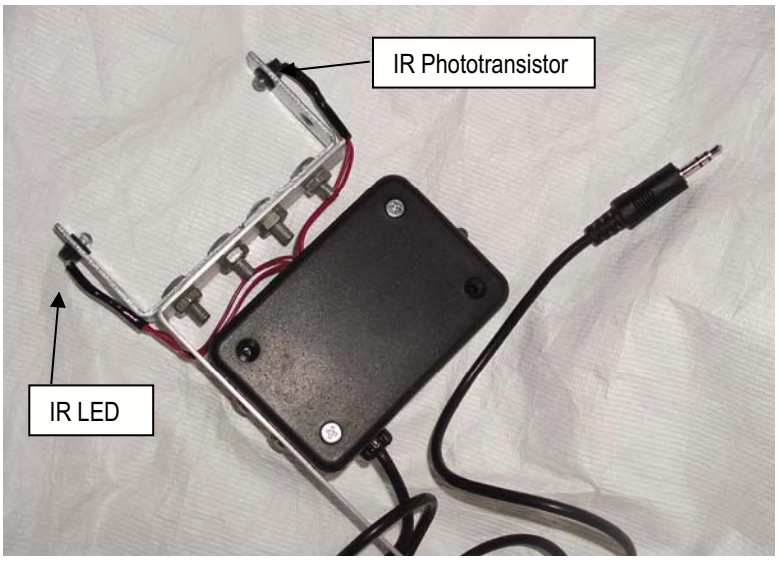

Figure 6 Fully constructed infrared photogate trigger

Delay Controller

The delay controller is the most complex unit in the high-speed photography system. It interprets signals from the trigger sensors, implements a preset delay over a wide range of timescales, communicates with the camera in several modes, and pulses the high-speed flashes. A variety of control features provides a high level of flexibility for the photographer. The delay controller is created from a combination of logic gates, multivibrators, flip-flops, high-speed count-down timers, and decoders, and utilizes both Transistor-Transistor Logic (TTL) and Complementary Metal Oxide Semiconductor (CMOS) integrated circuit technologies.

The delay controller consists of three separate circuit boards: the Input/Output (I/O) board, the countdown board, and the display board. The I/O board interfaces with the trigger, the camera, and the flash controller, and also connects to part of the user interface (switches, indicator lights, etc.) on the front of the delay controller box. The countdown board implements a delay on the order of microseconds to milliseconds and provides digital shutter

synchronization. The display board displays the four-digit number from the countdown board using a numeric seven-segment LED display.

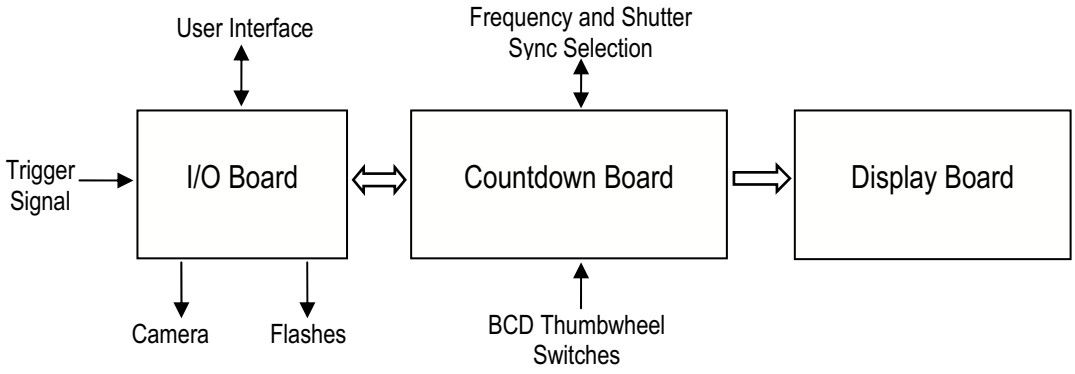

Figure 7 Delay Controller block diagram showing the three boards and their connections

Due to its complex nature, the delay controller was the last of the items in the high-speed system to be constructed.

Display Board

The display board is the simplest of the three parts of the delay controller and therefore will be covered first. The principle behind the display board is straightforward: to take a four-digit number represented in binary-coded decimal (16 channels of 1's and 0's) and translate it into a numeric representation that can be displayed on a four-digit numeric LED display, like the one shown in Figure 8.

Figure 8 A four-digit (seven segments per digit) numeric LED display

Binary-coded decimal, abbreviated BCD, is hybrid form of binary and decimal that is a convenient way to representing a decimal (base-10) number in binary (base-2).[8] Each decimal number place is represented by four binary number places. Table 1 charts the BCD encoding of decimal numbers 0 through 9.

BCD					Decimal Correspondent
Number	8's place	4's place	2's place	1's place	
0000	0	0	0	0	0
0001	0	0	0	1	1
0010	0	0	1	0	2
0011	0	0	1	1	3
0100	0	1	0	0	4
0101	0	1	0	1	5
0110	0	1	1	0	6
0111	0	1	1	1	7
1000	1	0	0	0	8
1001	1	0	0	1	9

Table 1 The encoding of decimal numbers 0-9 in BCD

The numbers 1010 through 1111 are invalid in BCD because they cannot be represented with one digit in decimal.[8] To represent larger decimal numbers, from 10 to 99, requires an additional four BCD places. Rather than corresponding to 16's, 32's, 64's, and 128's places, as these places would in standard binary, the four additional BCD places correspond to the 10's, 20's, 40's, and 80's place. Consider the representation of the decimal number 67 in BCD, as shown in Table 2.

BCD								Decimal Correspondent
Number	80's	40's	20's	10's	8's	4's	2's	1's	
0110 0111	0	1	1	0	0	1	1	1	67

Table 2 The BCD encoding of the decimal number 67

The delay controller is capable of handling any 4-digit decimal number from 0-9999, and requires the use of 16 BCD digits. BCD is a convenient and powerful tool. Computation of BCD numbers is the backbone of the digital delay controller in this high-speed photography system.

The display board schematic is shown in Figure 9. The display board receives a 4-digit decimal number (represented by 16 BCD digits) from the integrated circuits on the countdown board via 16 of the 20 parallel data channels on a 20 pin Insulation Displacing Connector (IDC), also known as a ribbon cable connector. Three of the remaining channels are used to power the display board (one wire is +5V, two wires are grounded), and the last channel is used to power the decimal point after the one's digit, which illuminates when the counter reaches 0000 and is used to calibrate shutter synchronization.

Four BCD-to-seven segment LED display decoders (IC number 4511) translate the BCD number into a pattern that can be displayed on a four-digit seven segment display.[9] As is standard practice with working with LEDs, because they exhibit a voltage drop but negligible resistance, the LEDs must be current limited with series resistors to prevent them from burning out. An array of twenty-nine (seven for each of the four numeric digits plus one for the decimal point) 330Ω resistors current limit the LED display and fix the display's brightness.

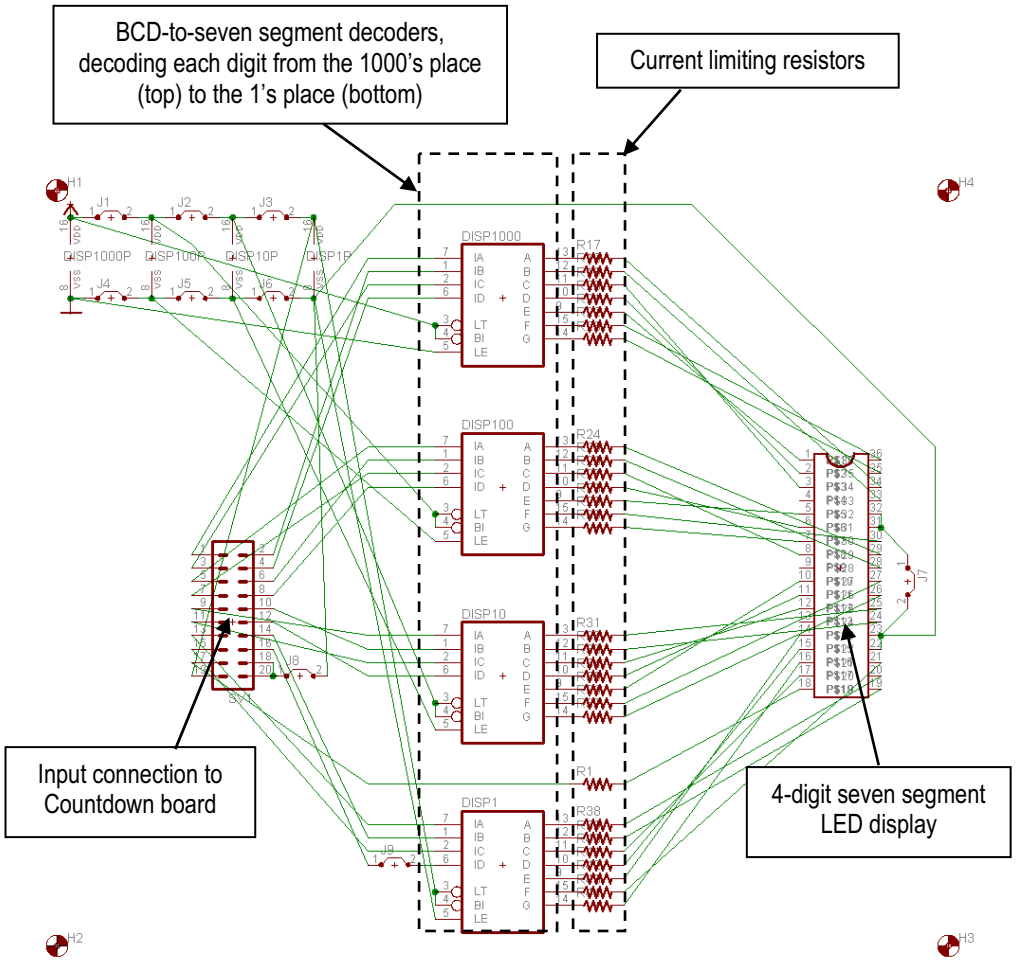

Figure 9: Display board schematic, designed using EAGLE CAD program

All of the circuit boards used in the delay controller and some of the circuit boards used in the high-speed flashes were designed using the computer-aided-design (CAD) program EAGLE. EAGLE allows for the design of circuit schematics and the translation of these schematics into PCB layouts.[10] A screenshot of the EAGLE board layout for the display board can be seen in Figure 10. The PCB layouts can then either be uploaded to PCB manufacturers for professionally made boards (at a cost of several hundred dollars per board design), or used to etch and create PCBs by hand.

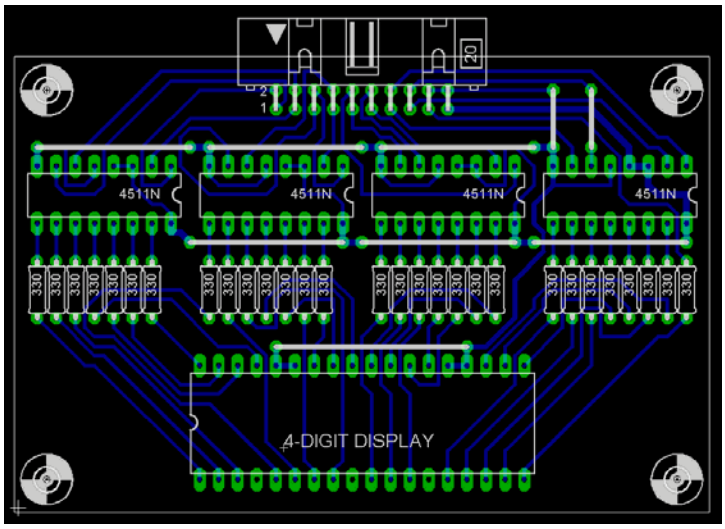

Figure 10 The display board physical layout in EAGLE, featuring the 20-pin IDC header at the top, the 4511 BCD-to-seven segment display IC's in the middle, followed by the current limiting resistors and the 4-digit display at the bottom.

In this case, all of the PCBs were created by hand using a toner-resist method. The PCB layouts, such as the one for the display board shown in Figure 11, were printed out using a laser printer onto special paper coated in a heat-resistant water-soluble polymer. The toner was fused to a copper-clad board (a board consisting of a non-conductive substrate with thin layers of copper laminated to the outside) by sandwiching the special paper with the toner design against the copper clad board and applying heat and pressure. The board and paper were then immersed in water, causing the paper's polymer to dissolve and the paper to separate from the board, leaving the toner pattern fused to the board. Next, the copper clad board was immersed in a vertical tank with a heated solution of ammonium persulfuate. The ammonium persulfate etched away the exposed copper within a matter of minutes, leaving only the copper traces protected by the toner mask.

Once removed from the etching tank, the toner was cleaned away with xylene, leaving the copper traces exposed. Using a product known as Cool-Amp, containing a mixture of sodium chloride, calcium carbonate, and silver chloride, a very thin layer of silver was applied to

the exposed copper traces to protect them from corrosion and increase conductivity and solderability. The etched board can be seen in Figure 12.

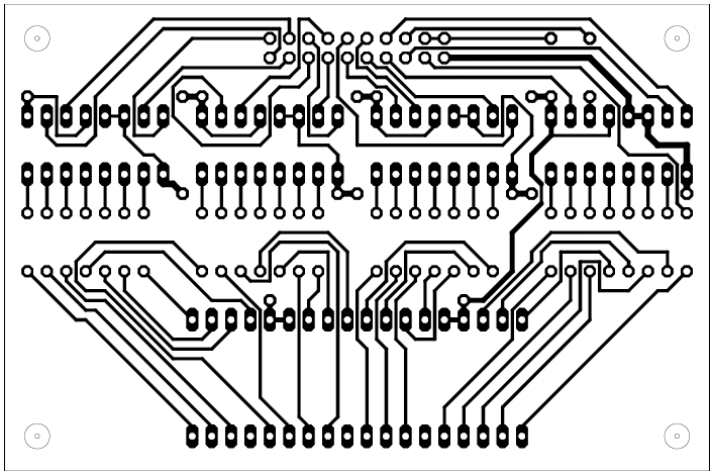

Figure 11 Pattern of traces (shown actual size) that was used to etch the Display board

Once etched and coated in silver, the display board was ready for drilling. Due to the nature of their small size, the holes in PCBs are best drilled with high-speed tungsten carbide bits designed for PCB manufacture. These bits, on the order of 0.050" diameter and smaller, were used with a Dremel® brand high-speed rotary tool mounted in a miniature drill press and operated at 10,000 rpm. Each hole drilled by hand. The excess PCB around the edges was trimmed with a sheet metal shear. The board was then ready for component installation.

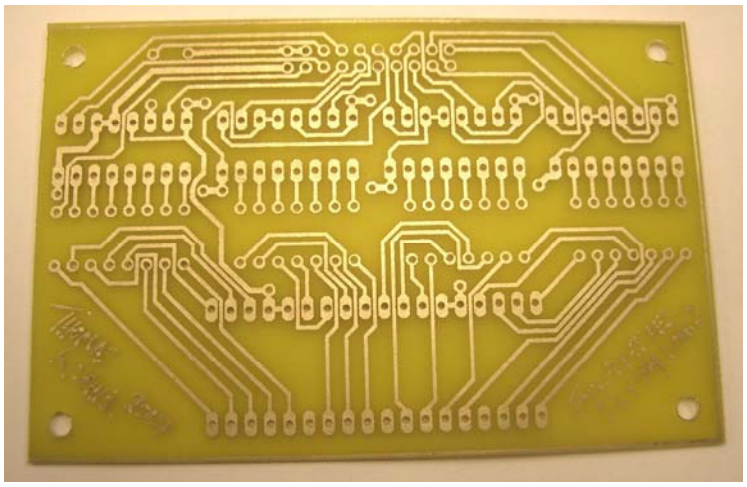

Figure 12 Display board after etching, silver coating, and drilling

Next, the board was soldered with components. The 20-pin IDC connector, current limiting resistors, and jumpers were soldered directly to the board. Machine pin IC sockets were soldered to the board and the ICs were press-fitted into the sockets. The sockets prevent the ICs from being heat damaged in the soldering process and also allow for the quick exchange of an IC if that IC were to become damaged. The completed display board is pictured in Figure 13.

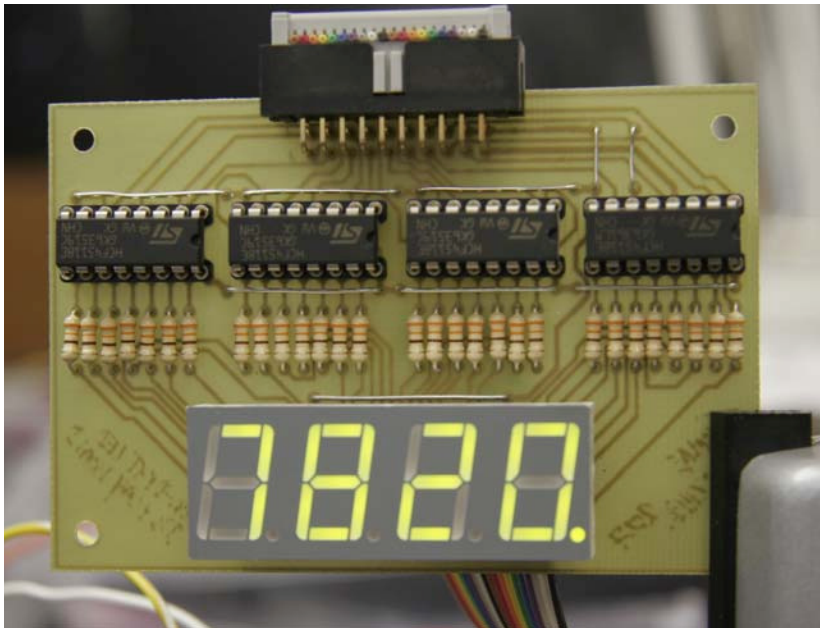

Figure 13 The completed display board

Countdown Board

Just as the delay controller is the most complex unit in the high-speed photography system, the countdown board is the most complex unit in the delay controller. The full schematic for the countdown board is shown in Figure 14. It will be explained in sections.

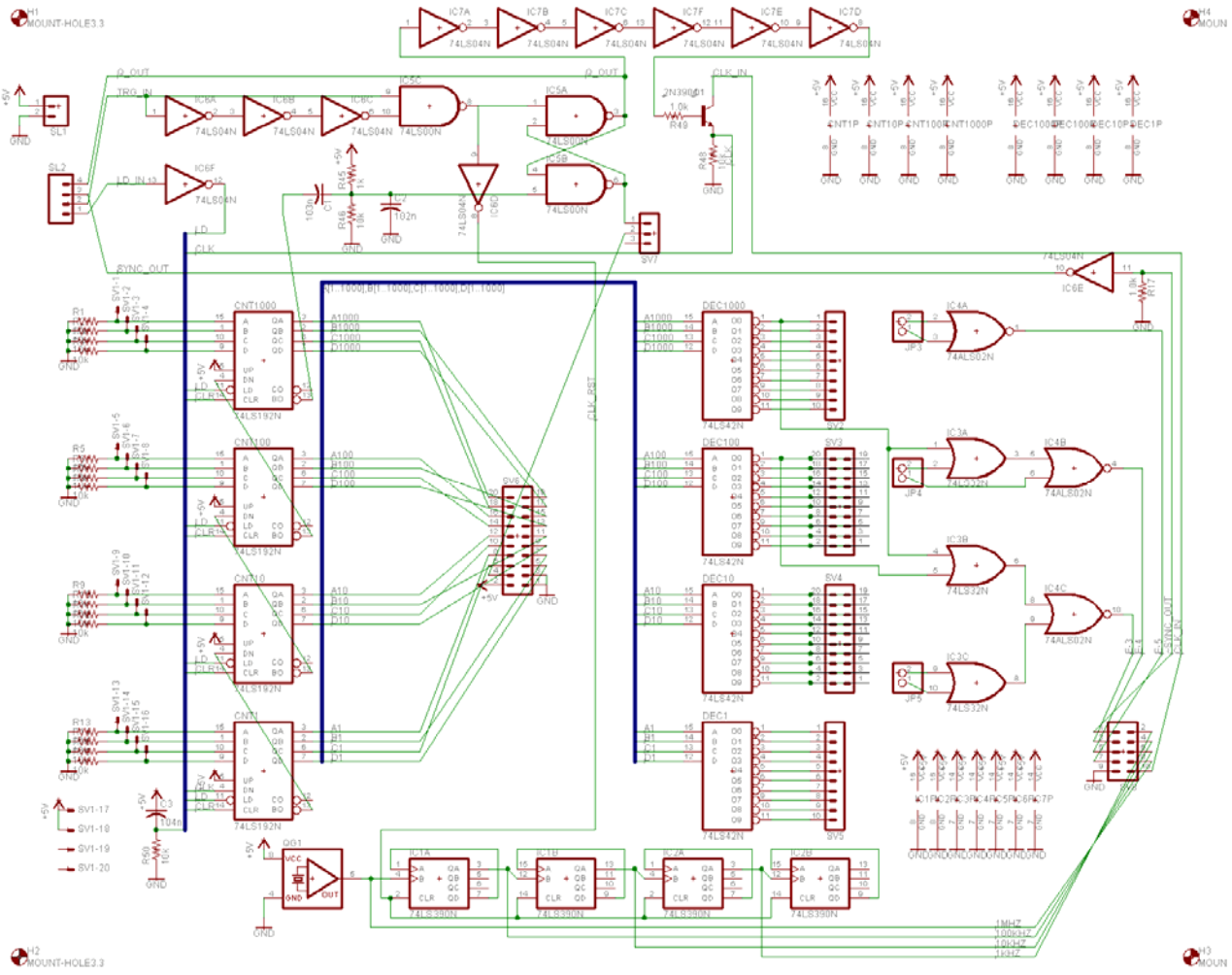

Figure 14 The complete countdown board schematic

The countdown board houses the backbone of the delay controller, the four stage BCD countdown timer ICs (shown in detail in Figure 20). These ICs are cascaded to countdown a four digit number and serve the primary purpose of the delay controller, to implement a preset delay.

The countdown board interfaces with the I/O board with a power input and a mere four signal channels, as shown in Figure 15. These channels are named LD_IN (number load input), TRG_IN (trigger input signal), SYNC_OUT (shutter synchronization output), and Q_OUT (countdown completion output).

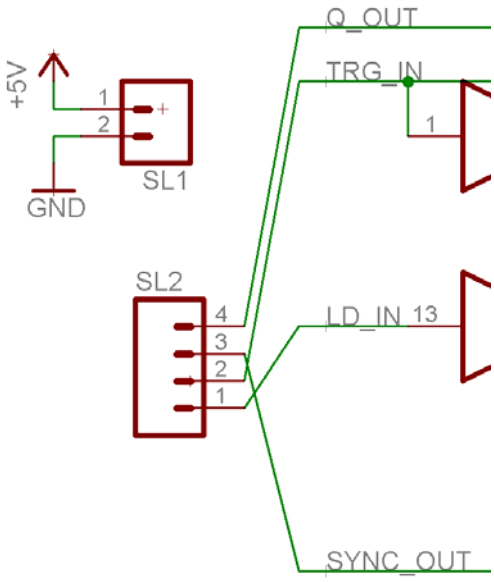

Figure 15 Power input and four channels for communicating with I/O board

The LD_IN number load input signal is activated when the photographer presses a reset button connected to the I/O board. It signals the four stages of the countdown timer to load the number on the BCD thumbwheel switches shown in Figure 16. When the reset button is pressed, the photographer will see four-digit LED display board switch from 0000 to the number shown on the front of the BCD thumbwheel switches.

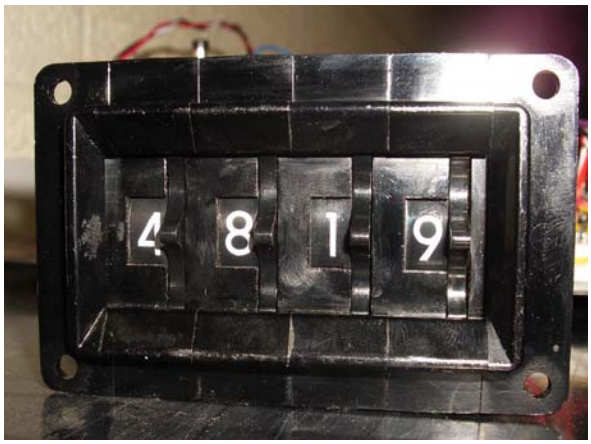

Figure 16 The BCD thumbwheel switches used for loading a number into the countdown timers. Although somewhat dated, in this circuit the thumbwheel switches require far less peripheral circuitry than a keypad would. The switches also make it convenient to tune the delay in increments of 1, 10, 100, or 1000.

The TRG_IN trigger input signal is a signal that goes high when delay controller receives a signal to begin counting down a delay. However, this trigger signal goes high and remains high, so it must be converted into a brief pulse to prevent the countdown timers from recycling when they reach 0000.

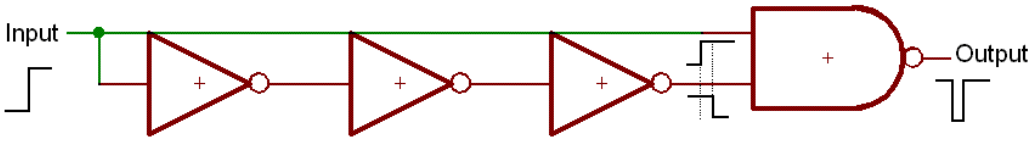

Figure 17 The NAND gate differentiator: a novel method for convert a rising edge into a negative pulse by exploiting inherent propagation delay in logic gates[11]

This brief pulse is created by implementing a NAND gate differentiator, shown in Figure 17. When the input to this system is low, the top NAND gate input is low, but the bottom NAND gate input is inverted, and thus high. When the input signal goes high, the top NAND gate input immediately goes high as well, and the bottom NAND gate input remains high while

the input signal change propagates through the three inverters. The NAND gate responds with a low output. After about 30ns, the time it takes for the signal change to propagate through the inverters, the output of the last inverter goes low, and the NAND gate output goes high once more.[11]

The brief negative pulse output of this circuit is a negative "differentiation" of the rising edge input signal. This is a very useful circuit for edge triggering; it produces a clean pulse that is more stable and predictable than capacitor differentiation of signals. By replacing the NAND gate with AND, OR, or NOR gates, any of the four combinations of positive or negative differentiation of rising or falling edges can be obtained. The differentiated pulse is also used to reset the frequency dividers in the frequency generator circuit, thus provided additional timing accuracy.

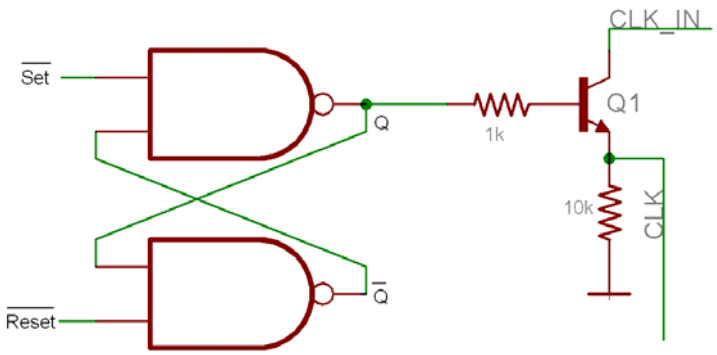

Figure 18 NAND gate SR latch connected to transistor Q1 gating clock signal

Next, the "differentiated" output triggers the NAND gate Set-Reset (SR) latch, shown in Figure 18. The pair of NAND gates with feedback form a bistable multivibrator, otherwise known as a latch. The truth table for the SR latch is shown in Table 3.[12] Note that both inputs can never be low at the same time, as this would correspond to an unpredictable output. Good mechanical analogs to the set-reset latch inputs are the "play" and "stop" switches on an audio cassette player.

$\overline{\text{Set}}$	$\overline{\text{Reset}}$	Q	$\overline{\text{Q}}$
1	1	Latch	Latch
0	1	1	0
1	0	0	1
0	0	Invalid input	

Table 3 NAND gate SR latch truth table

When the SR latch is set, the Q output goes high. The Q output is connected to the base of transistor Q1 (not to be confused with the Q output of the SR latch), as shown in Figure 18, which causes the transistor to conduct and pass the clock signal from CLK_IN to CLK. The clock signal on CLK becomes the base frequency for decrementing the number loaded into the digital countdown ICs, and thus implementing the delay.

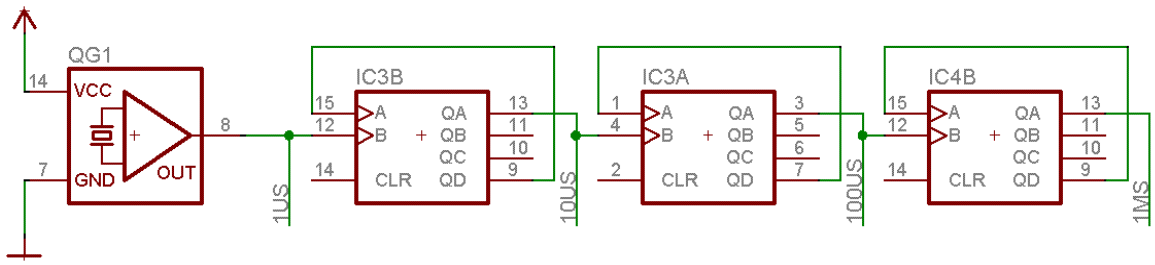

Figure 19 Clock generator featuring oscillator and frequency dividers

Figure 19 shows how the four clock signals are generated. A 1.000 MHz TTL square-wave crystal oscillator is connected to a series of divide-by-10 ICs (part number 74LS390) that reduce the clock frequency in stages[13]. With a rotary switch, the photographer can select the clock signal that is connected to the countdown timers to be 1 MHz (an undivided signal), 100 kHz, 10 kHz, or 1 kHz.

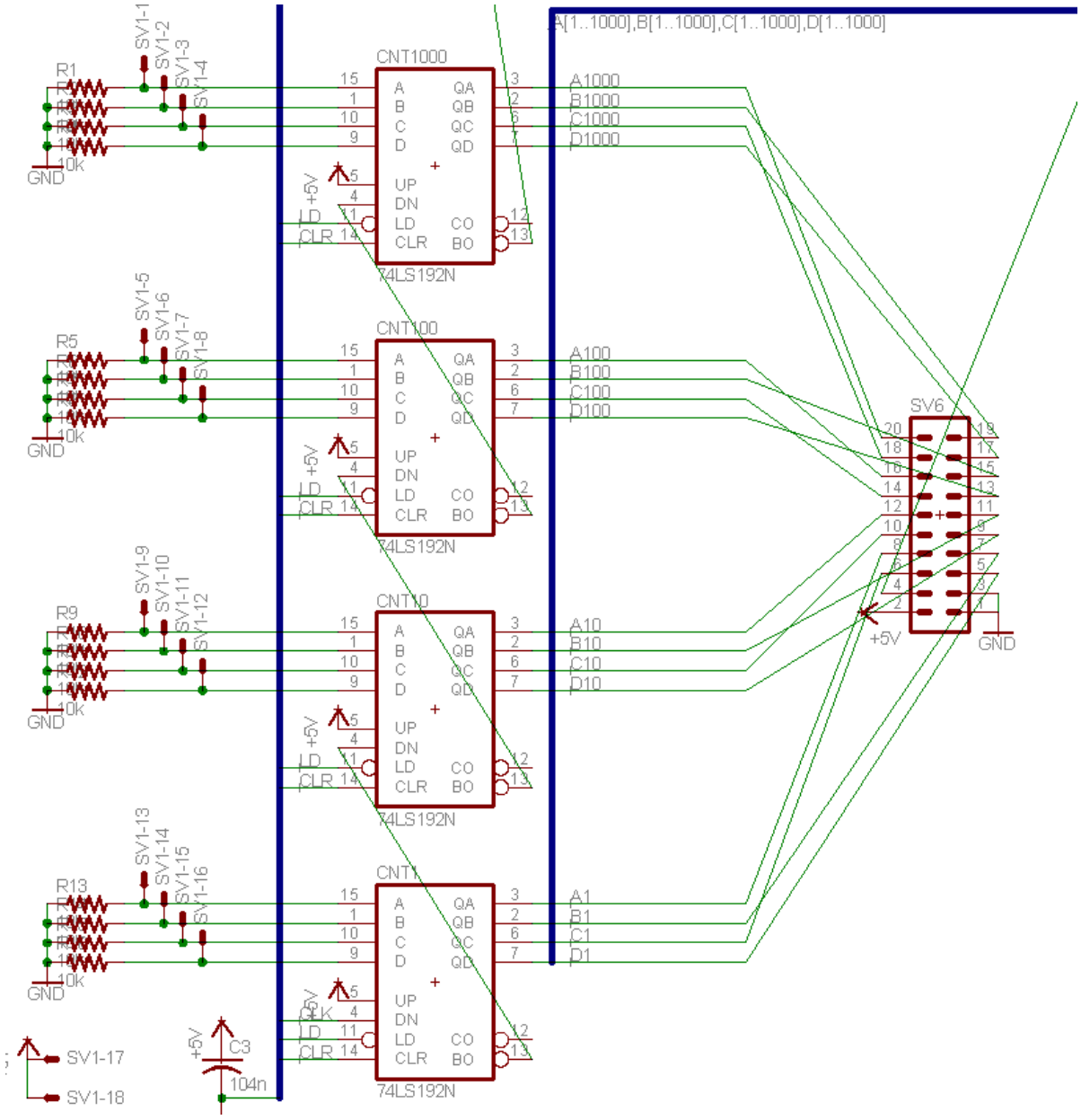

Figure 20 Cascaded BCD countdown timers (74LS192)[14] shown in the middle. They are flanked on the left by the connector to the BCD thumbwheel switches (SV1-1,2,3,etc) with pull-down resistors, and on the right by the connector to the display board (SV6). The thick blue lines are busses, which take the place of individual wires and make a prettier and easier-to-read schematic.

The gated clock signal from the emitter of Q1 enters the least significant digit of the BCD countdown timers. It enters on pin 4 of CNT1 timer, shown at the bottom of Figure 20. On each rising edge of the clock signal, the CNT1 BCD timer decrements the number stored in its

register. When CNT1 reaches zero, it emits an output pulse on B0 (pin 13), which is connected to the down clock input of CNT10, the ten's place counter. The process of connecting the terminal count outputs of each digit to the down clock inputs of the next higher significant digit is called cascading. All four digits are cascaded by the diagonal wire connections illustrated in Figure 20.

When all four digits reach zero, the terminal count down (pin 13) of the thousands place counter falls. This falling edge is differentiated by capacitor C1 shown in Figure 14 to create a negative pulse that resets the NAND gate SR latch. When the SR latch is reset, the Q output of the NAND gate SR latch goes low and transistor Q1 no longer conducts the clock signal. No longer receiving any clock signal, CNT1 ceases decrementing and the output of the four counters remains frozen at 0000. The reset of the SR latch also causes the signal Q_OUT to go low, which signals the I/O board to fire the flashes.

The countdown board also hosts the delay controller's feature of shutter synchronization. Shutter synchronization is the ability to time the opening of the shutter with the firing of the flashes. This allows the photographer to use much faster shutter speeds and also affords the photographer greater flexibility photographing in environments with ambient light, such as outdoors during daytime rain, or in a moderately lit room. In the history of high-speed photography, almost all work has been done in darkened environments, with camera shutter open for long periods of time and with the high-speed flash providing the only source of illumination for the scene. Without shutter synchronization, only objects within a close range of the flash are illuminated and the background remains underexposed, as exemplified by the photo in Figure 21.

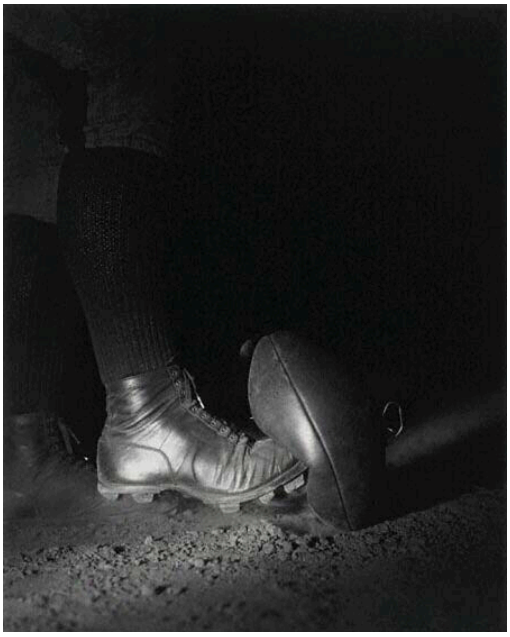

Figure 21 Edgerton's "Wes Fesler Kicking a Football"[15] illustrates the limited foreground illumination characteristic of a system without the capability of shutter synchronization.

The shutter synchronization feature in this high-speed system allows the photographer to synchronize the opening of the shutter with the firing of the flash at shutter speeds as fast as 1/250 of a second.

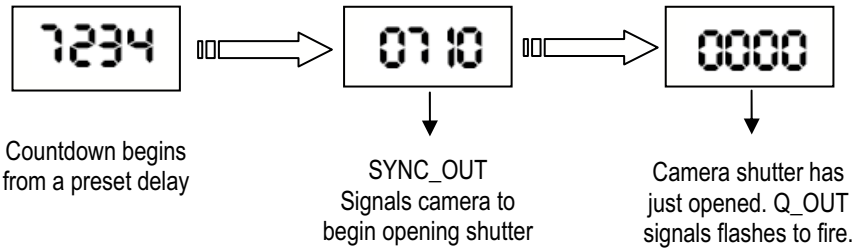

Figure 22 Implementation of a 71 millisecond shutter synchronization with a countdown timer base frequency of 10 kHz.

The feature of shutter synchronization begins with BCD-to-decimal decoders (IC number 74HC42). These ICs are connected to the BCD outputs of the counters, the same outputs to which the BCD-to-seven segment decoders on the display board connect. The BCD-to-decimal

decoders convert a BCD input into a negative-logic output on one of ten different pins, as shown in Figure 23, corresponding to decimal digits 0-9. For example, when the BCD-to-decimal decoder reads a BCD input of 0111, it outputs low on its 7's place (pin 9) while the other nine output pins remain high. The ten outputs from each of the four BCD-decimal decoders are then connected to male headers. Figure 26, the completed countdown board, shows the male headers as gold pins sticking out from the circuit board.

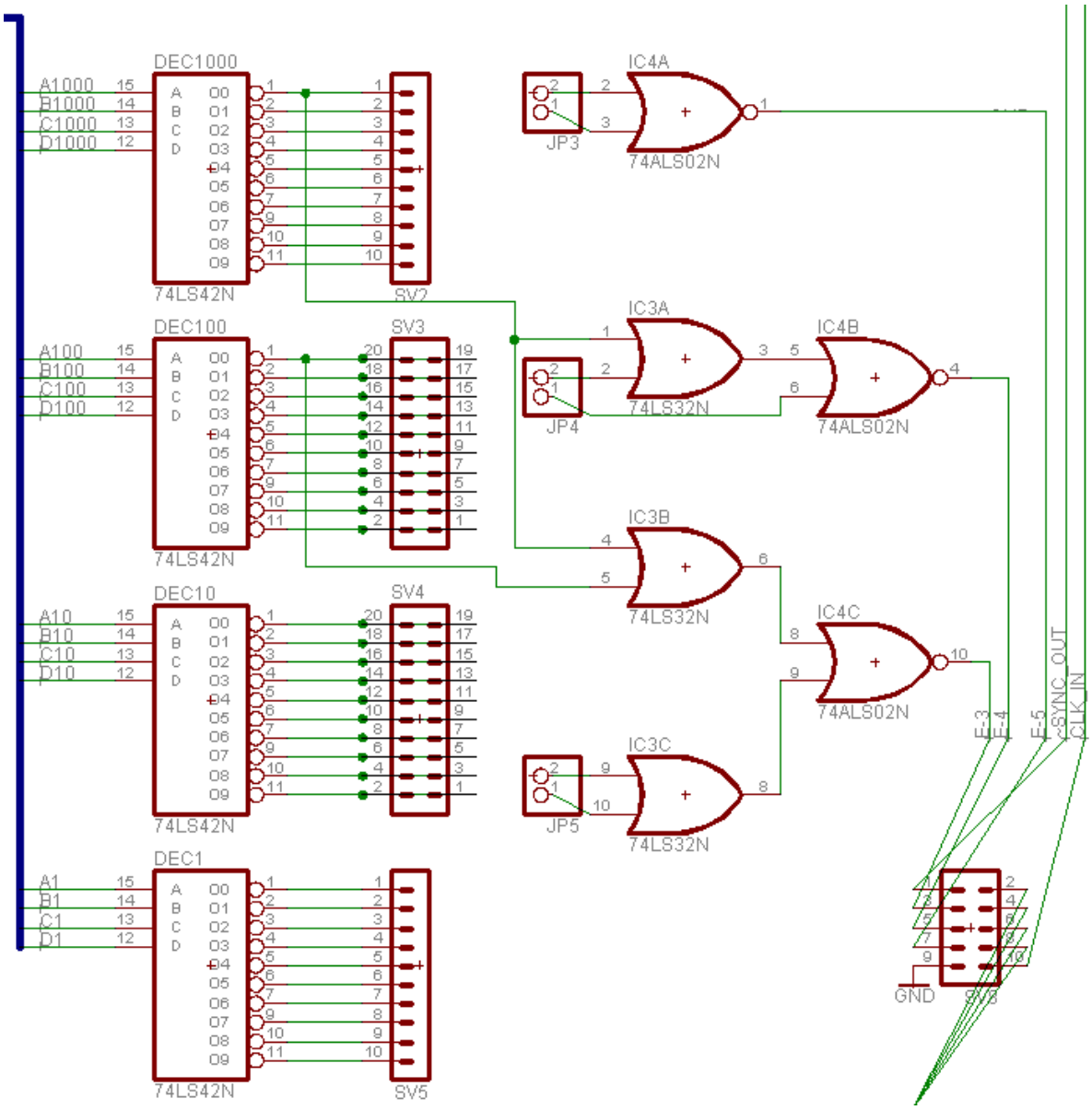

Figure 23 The shutter synchronization circuit. The BCD-to-decimal decoders are shown at the left, followed by the male pin headers, the three two-pin headers, and the OR and NOR gates. The ten-pin IDC connector to the rotary switch, which also provides clock signal selection, is shown at the bottom right.

The system for selecting a given shutter synchronization delay then relies on a point-to-point wiring method to anticipate the shutter lag before the counter reaches 0000 (refer to Figure 22). Shutter lag refers to the time lag between signaling the camera to take a picture and the shutter opening. This lag is primarily due to physical processes in the camera (the mirror

moving). In this case, it was experimentally determined that the camera being used, a Canon digital single lens reflex (dSLR) EOS 20D, has a shutter lag of 71ms. This measurement was made by initially programming a shutter lag of 65ms (the specification given by the manufacturer), aiming the camera at the 4 digit display with the flash nearby, and gradually increasing the delay until the flash could be seen in the picture. Using wire connectors, the photographer can select a two digit number (for each clock frequency) that corresponds to the shutter lag of the camera used. This must be done for each of the three two-pin headers (each set of two pin headers is necessary for the different frequencies of 1kHz, 10kHz, and 100kHz).

Consider the example of programming in a shutter lag of 71ms for the base frequency of 1kHz. Referring to the schematic in Figure 23, the photographer would use wire jumpers to connect pin 2 from JP5 to pin 5 of SV4, and pin 1 of JP5 to pin 2 of SV5. Thus, when the countdown sequence reaches 71ms, DEC10 will output low on it's "7" output (pin 9), and DEC1 will output low on it's "1" output (pin 2), causing the OR gate IC3C to go low. The addition of the OR gate IC3B that is connected to the "0" outputs of DEC1000 and DEC100 ensures that there must be leading zeros in the seconds and tenths-of-second places when the shutter fires at 71ms. This is because both inputs to the NOR gate IC4C must be low in order for the NOR gate to emit a positive pulse of 1ms duration when the count is 0071.

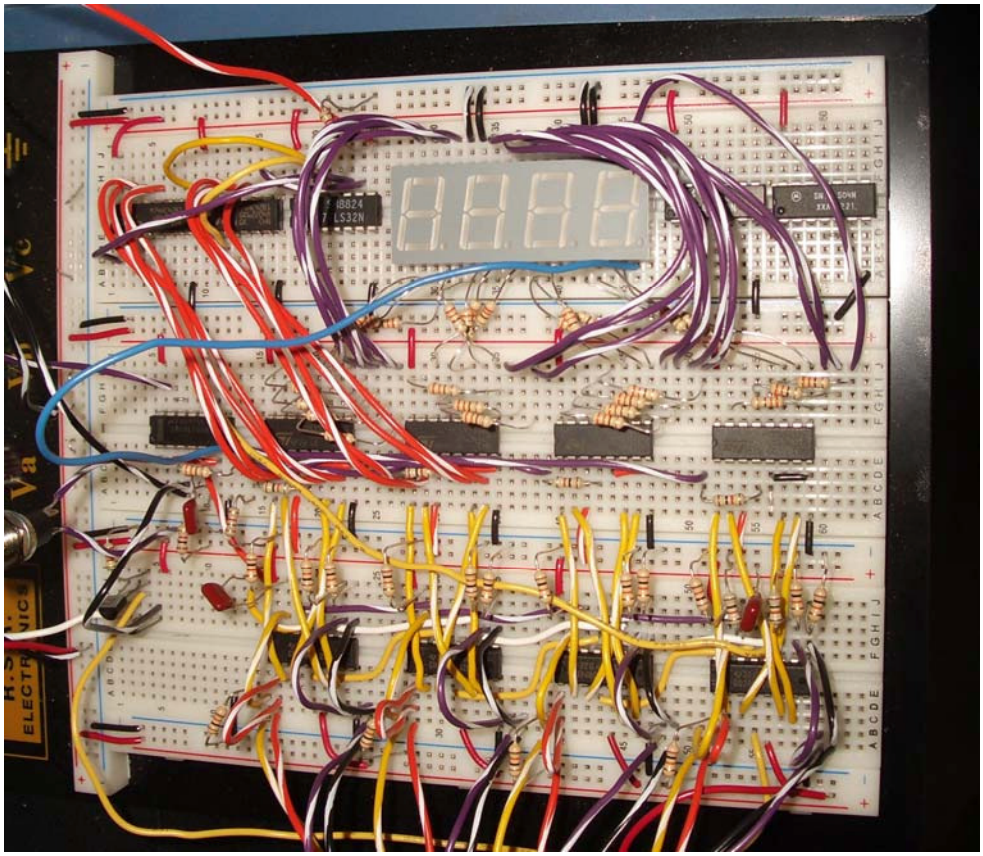

Figure 24 The prototyped countdown board and display board. The wires coming off of the bottom of the breadboard connect to the BCD thumbwheel switches.

When the number in the counters corresponds to the selected shutter lag, the series of OR and NOR gates drawn in the Figure 23 schematic creates an output pulse on the wire SYNC_OUT, which signals the I/O board to fire the camera. Over the next 70ms, as the camera begins the process of opening the shutter, the counter continues to decrement towards zero. Then, roughly a millisecond before the counter reaches zero, the camera shutter opens and exposure begins. While the shutter is open, the counter reaches zero, the flash fires, and the shutter closes soon thereafter.

With the option of shutter synchronization, the photographer will not have to work in the complete darkness (a major advantage) and will also have the ability to expose the background in

photos, which is especially useful when shooting in an outdoor environment. Shots such as a raindrop hitting a flower with a landscape in the background become possible.

The breadboard prototype for the countdown board and the display board are shown in Figure 24, without the complete shutter synchronization circuit. Once the display board was successfully created, the corresponding parts of the display controller board were removed from the breadboard.

Figure 25 illustrates the EAGLE CAD layout for the countdown board. Note that due to the complexity of the countdown board, it was necessary to create a double-sided PCB. As of April 22, 2007, the permanent version of the countdown board, as shown in Figure 26, has been created and is fully operational.

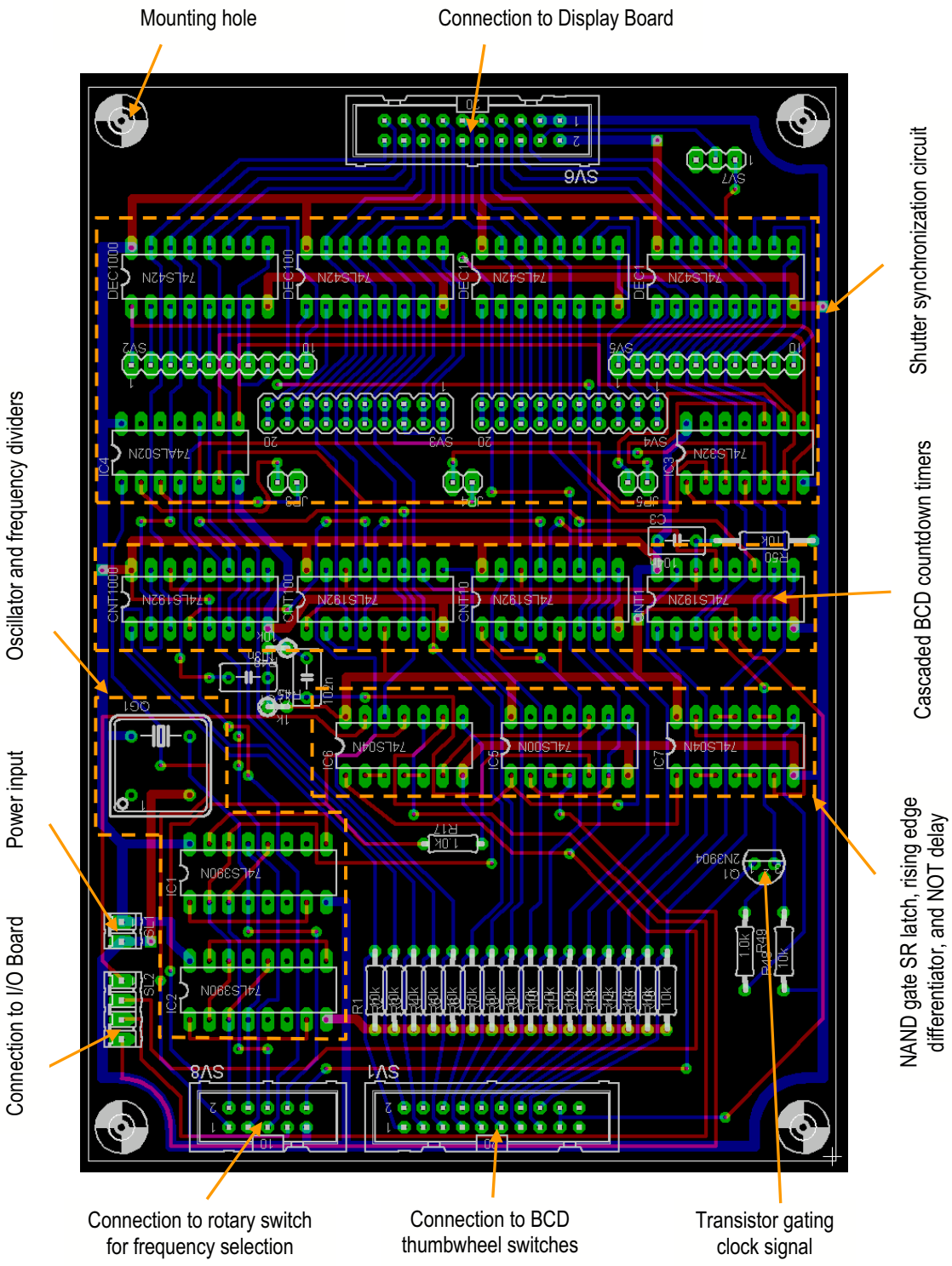

Figure 25 Annotated layout of countdown board

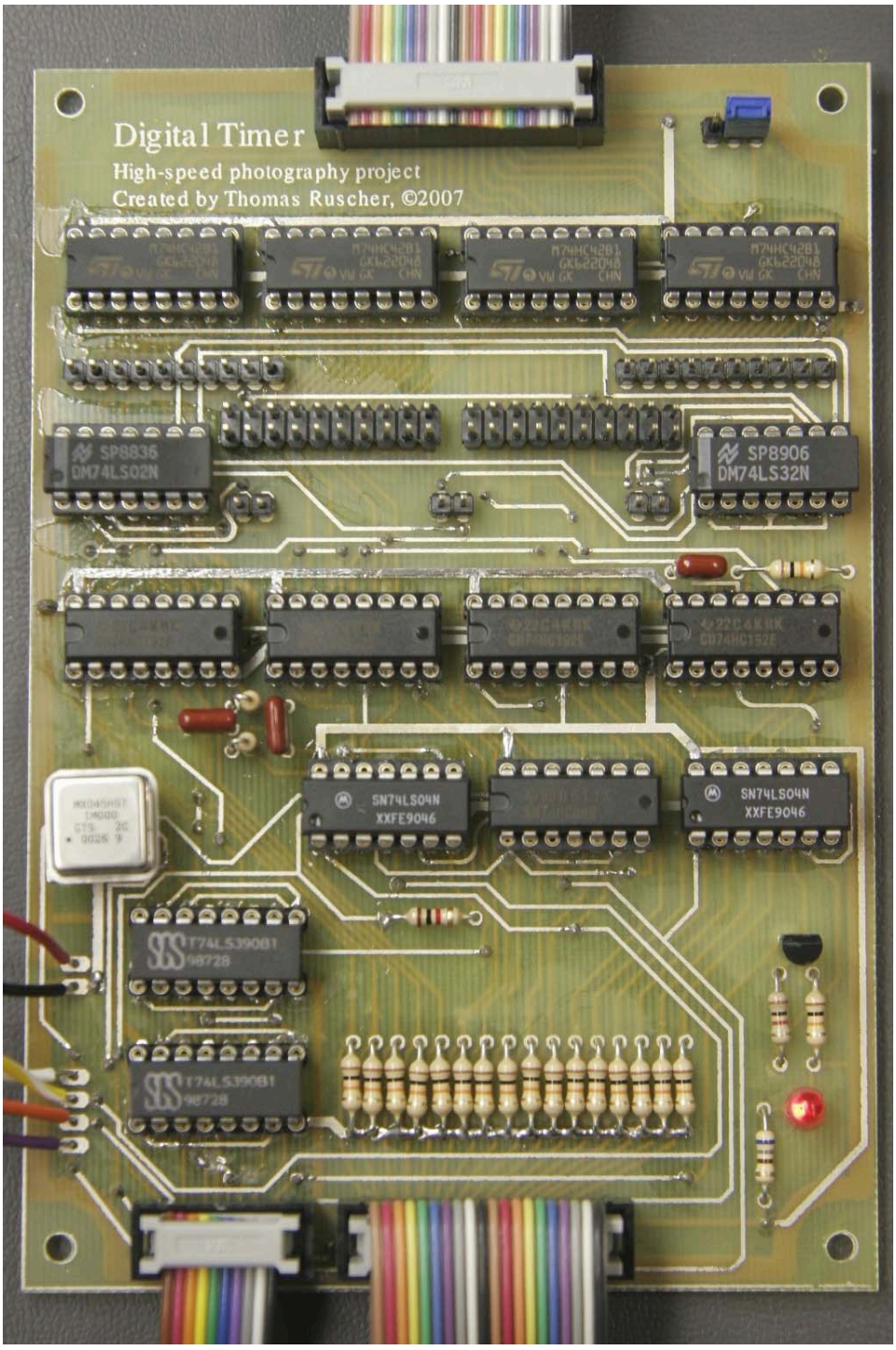

Figure 26 The completed, fully operational countdown board. (125% actual size)

I/O Board

The I/O board interfaces the delay controller with the other components in the high-speed system: the trigger, the flashes, and the camera. The I/O board is a hub, mediating signals between components. For this reason, I/O board was the last circuit board in the delay controller to be built, because it must effectively communicate with the other components.

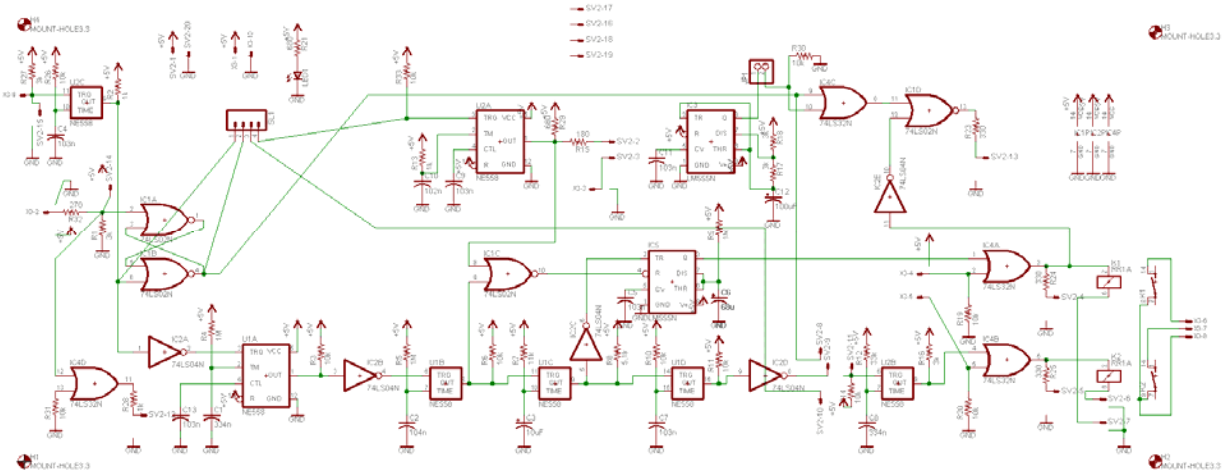

Figure 27 I/O board schematic

Figure 27 is the schematic diagram for the I/O board. The I/O board accepts a digital signal pulse from the trigger that connects to the delay controller box using a standard 3.5mm stereo headphone jack. The trigger signal becomes the input to a positive-logic set-reset (SR) latch, consisting of a pair of NOR gates with crossed feedback. The SR latch allows only one trigger signal at a time to affect the system. After the NOR gate SR latch has been set by the rising edge of a trigger signal, it can only be reset by photographer pushing a reset button. This feature prevents the delay controller from behaving erratically when there are an excessive number of trigger events, for example, many water drops falling.

Most of the I/O board consists of a series of one-shot delays (eight of them) that perform various functions. Six of the one-shot delays are needed to communicate with the Canon 20D camera, which behaves like a black box with regard to its focus and shutter operation. The camera needs certain minimum delays between the start of focusing and shutter activation. These delays were determined experimentally when the I/O board was prototyped on the breadboard. Of the two remaining one shot delays, one is used to debounce the reset switch, and the other is used to generate a microsecond duration pulse that triggers the flash controller. Another 555 timer is operated in astable (oscillating) mode and is used to create a flashing "system ready" LED indicator.

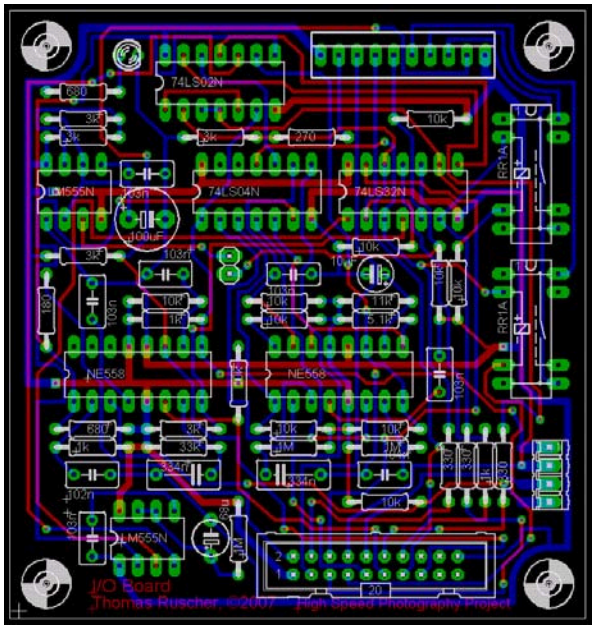

Figure 28 EAGLE CAD board layout for the I/O board.

Figure 28 and Figure 29 show the development of the I/O board from EAGLE layout to etching, soldering, and component installation.

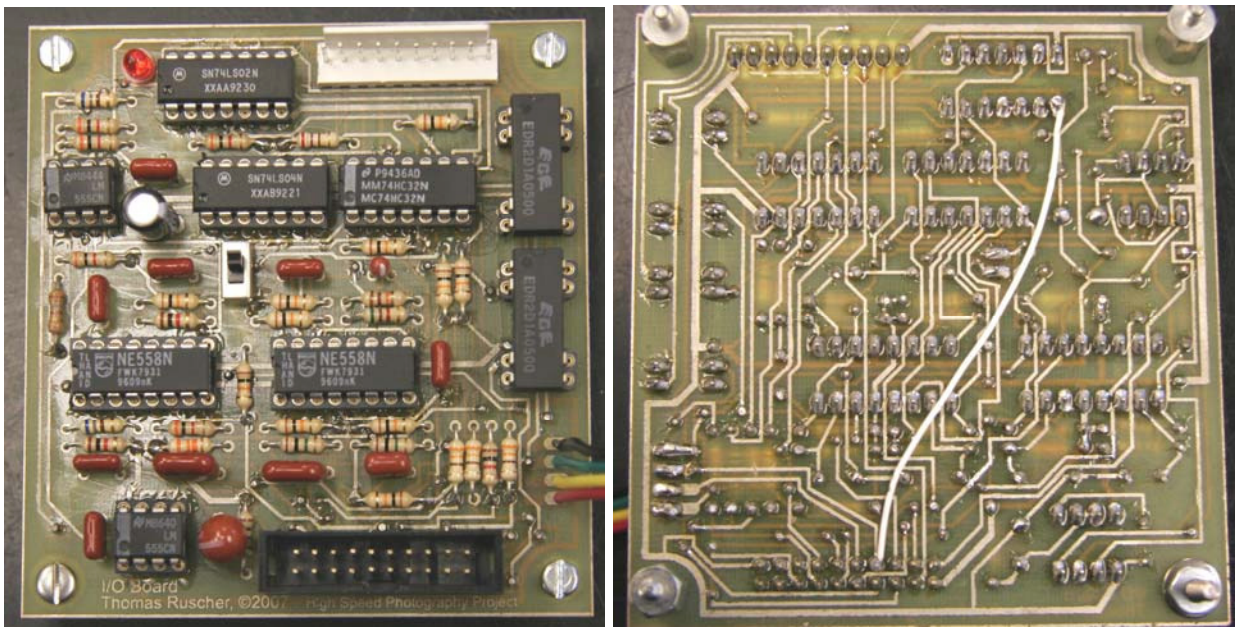

Figure 29 The top and bottom sides of the I/O board, pictured close to actual size On the bottom side, notice a mistake in the circuit that had to later be corrected with a wire jumper.

In a controlled setup with repeatable trigger events, the precision of the delay controller, show in completed construction in Figure 30, is instrumental in analysis of each possible moment. For instance, the terminal velocity of a large rain droplet is approximately 9m/s[16]. The ability to capture the event and discriminate between moments that are tenths or even hundredths of a millisecond apart (corresponding to millimeters or 10^{-4} m, respectively) will allow the photographer to perform a detailed study of the fluid dynamics of water collision, producing both artistically pleasing and scientifically significant images.

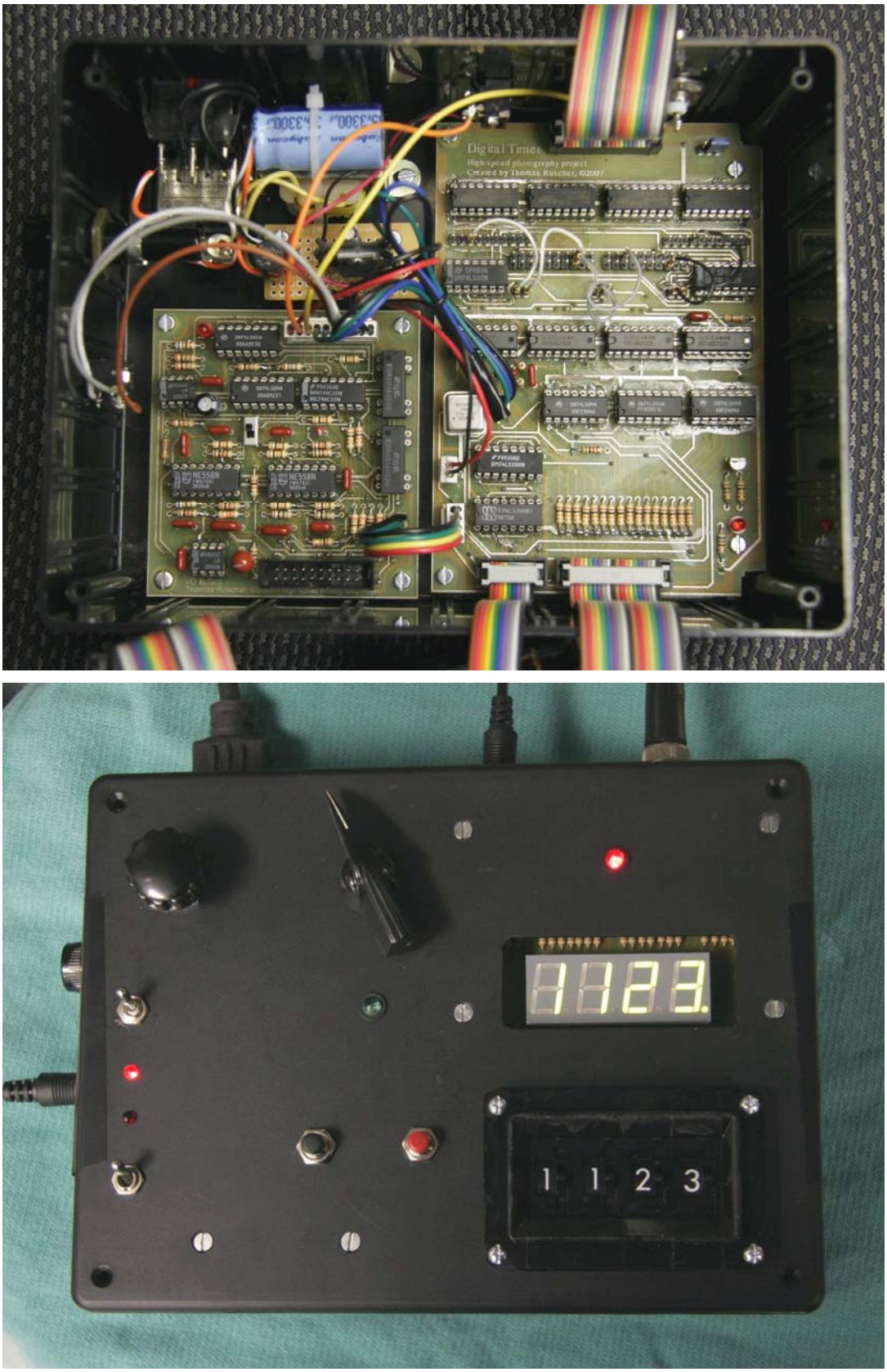

Figure 30 The completed delay controller internal view (top) and front panel (bottom).

Flashes

The high-speed flashes consist of two main components. The flash controller translates the signal from the I/O board of the delay controller into a pulse that can fire the flashes. The flash controller also supplies line current to the flashes. The flashes convert the line current into high voltage DC which is used to charge capacitors that fire the flash when the signal is received.

Flash Controller

Figure 31 shows the completed flash controller, which is an intermediary between the delay controller and the high-speed flashes. The flash controller electrically isolates the delay controller from the high voltage present within the flashes, controls multiple flashes (up to five), and serves as a power supply for the flashes, providing them with a fused source of 120VAC. The internal circuitry of the flash controller consists of a 6N137 high-speed optoisolator, a 555 timer, and a regulated 5VDC power supply.

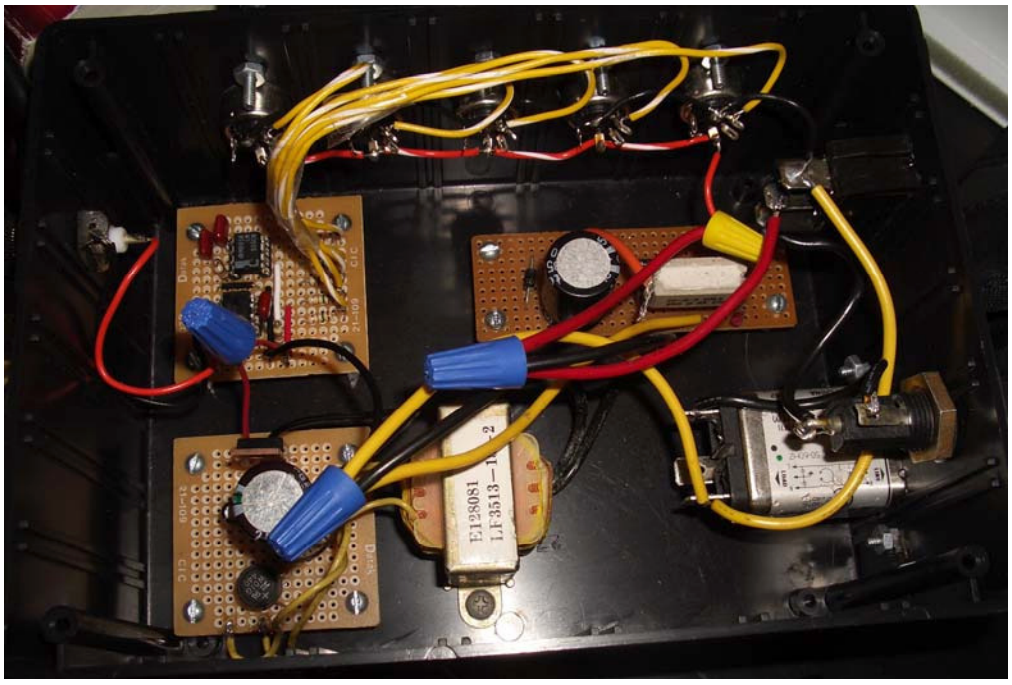

Figure 31 An internal view of the flash controller

High-Speed Flashes

The flashes' brief duration is the crucial element in freezing the subject in space. Typical commercial and consumer photographic flashes have durations ranging from 0.05 to 10 milliseconds. The flash system built in this project has a duration of less than 10 microseconds when operated at 900V and 2µF (refer to the graph in Figure 34).

The flash circuit in Figure 32 consists of several major parts, including the high voltage source, the photoflash capacitors, the xenon tube, and the trigger circuit. The luminosity of the flash discharge is proportional to *U*, the energy stored in the photoflash capacitors (given by Equation 2) multiplied by an efficiency constant *k* that depends on many parameters. The value of *k* is often so indeterminate that flash manufacturers specify the intensity of in terms of the energy stored in the photoflash capacitors, *U*.

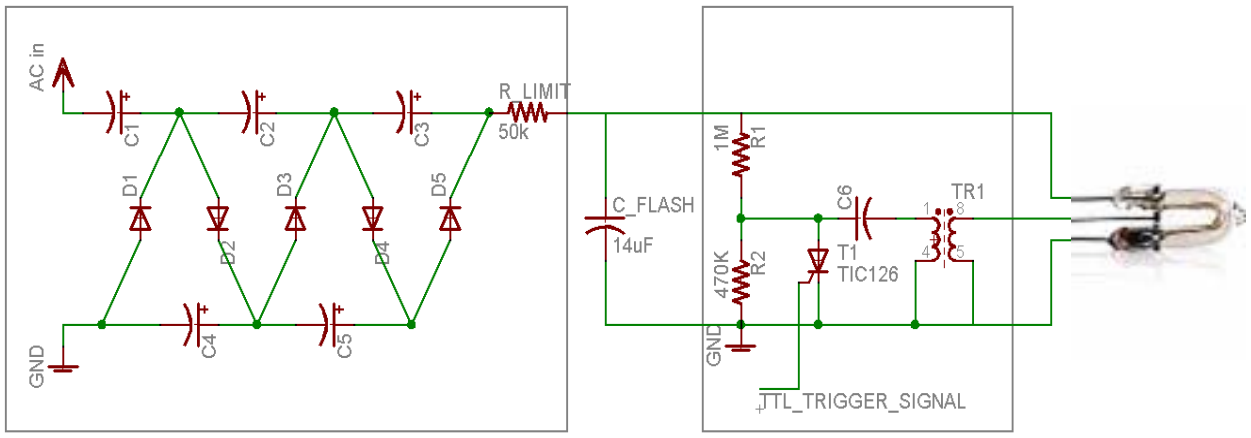

Figure 32 The high-speed flash circuit in four parts

The high-speed flash circuit works in the following manner: The Cockroft-Walton high voltage power supply charges the photoflash capacitor through the current-limiting series resistor R_LIMIT. The charging rate of the capacitor is determined by the time constant (Equation 1) for a series RC circuit. The capacitor is fully charged within seconds. Discharge of the flashtube

cannot occur until the xenon is triggered into conduction by an external high voltage pulse on the order of several kilovolts. This pulse is generated in the trigger portion of the circuit, which is operated by a 5V external pulse. Once triggered, the xenon flashtube conducts, and the only factors limiting the rate of discharge are the non-linear resistive properties of the xenon gas (determined by characteristics of the flashtube), the resistance and inductance of the connection between the flashtube and the capacitor, and properties of the photoflash capacitor.[17]

To lower the duration of a flash, an important goal in high-speed photography, one must raise the voltage and decrease the capacitance of the photoflash capacitors, which obey the energy storage relationship[18]:

$$U = (1/2)CV^2 \tag{2}$$

Conventional flashes operate in the region of 250-400V, with capacitances of several hundred or thousand microfarads. The flash currently in operation uses a voltage of 900V, with capacitance that can be varied between 2 and 14 microfarads, yielding a maximum energy of approximately 5J. Since most conventional flashes with longer durations have energies higher than this value, a significant limitation of our high-speed flash is that it must be used within close proximity of the subject to ensure adequate illumination of high-speed events.

The high voltage circuit used to charge the capacitors is based on the Cockroft-Walton voltage multiplier, which consists of a ladder arrangement of capacitors and diodes as shown in Figure 32. A major advantage of this circuit is that it can be operated directly from 120VAC 60Hz line current, eliminating the need for bulky step-up transformers. The maximum voltage output of the Cockroft-Walton multiplier is given by[19]:

$$V_{\max out} = 2 \cdot N_{stages} \cdot \sqrt{2} \cdot V_{in(RMS)} \tag{3}$$

Each stage (N_{stage}) consists of two capacitors and two diodes. On each positive oscillation of the voltage source, current is forced further up the "ladder", resulting in the simultaneous multiplication, rectification, and DC smoothing (filtering) of the power. However, as the load increases on the output of the multiplier, there is a corresponding voltage drop on the output which has dependence on current draw (I), input frequency (f), stage capacitance (C), and number of stages (N), according to the following relationship[19]:

$$V_{drop} = \frac{I}{2\pi fC}\left(4N^3 + 3N^2 - N\right) \tag{4}$$

The voltage output of the multiplier at any given time is then:

$$V_{out} = V_{\max} - V_{drop} \tag{5}$$

Design parameters were considered and a voltage multiplier was designed with 2-½ stages (five capacitors, five diodes) using 33µF 450VDC capacitors and 1N4007 general purpose 1A 1000V diodes for a max output voltage of 850-900V. A 50kΩ current limiting resistor on the output sets the maximum voltage drop of the divider to be approximately 200V, when the output is short circuited. This condition occurs the instant the photoflash capacitor is charged from zero potential, following a discharge. The maximum charging current in this instance is approximately 18mA, as calculated using the RC series circuit capacitor charging relationship given by[18].

$$I = \frac{V}{R} e^{\frac{-t}{RC}} \tag{6}$$

As voltage across the capacitor increases, less current flows through the series resistor, and the voltage output of the multiplier circuit increases. Within 5 seconds, the 14μF photoflash capacitor is at 99% of full charge.

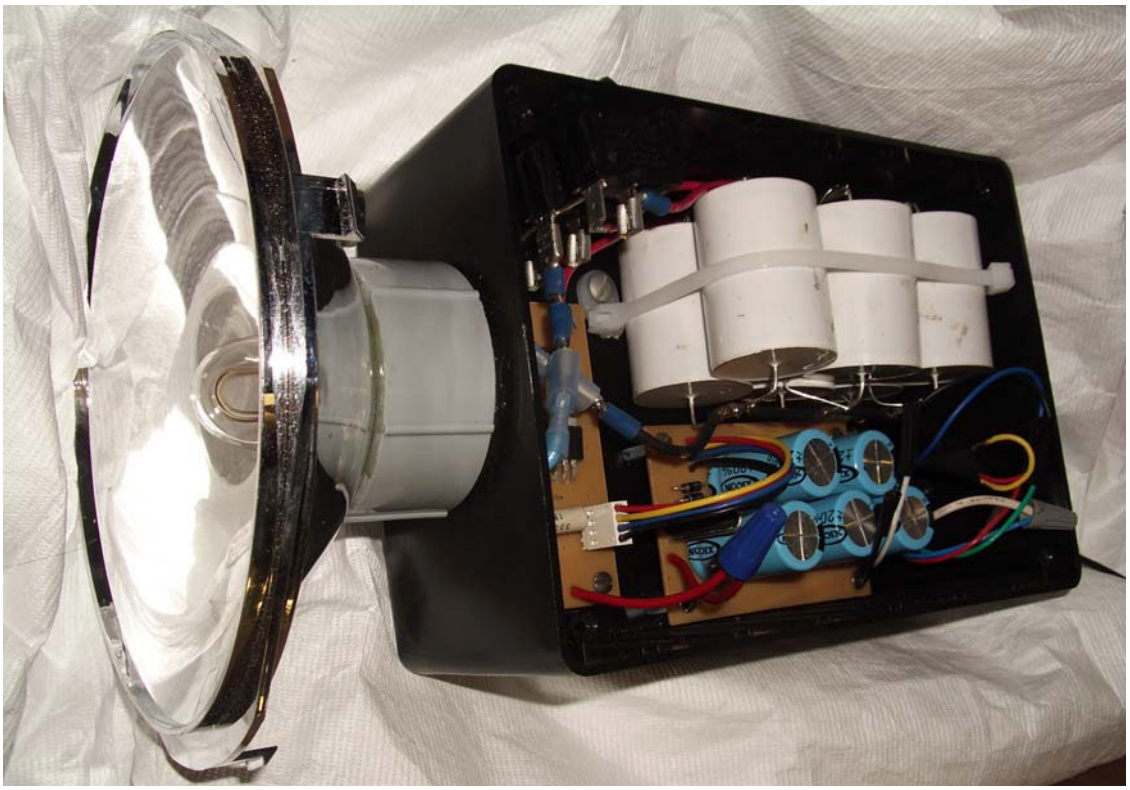

Figure 33 Completed high-speed flash. Note the Cockroft-Walton circuit (with blue electrolytic capacitors) in the lower right of the box, the bank of six1kV 2μF photoflash capacitors (white), the trigger circuit to the left, and the xenon flash tube and removable parabolic reflector protruding from the box.

The photoflash capacitor is a critical element in the flash circuit. It must slowly charge, and then dump all of its energy into the xenon tube on the timescale of microseconds. The capacitor must be chosen to have high current capabilities. High equivalent series resistances (ESL) could cause ohmic heating that would limit the rate of discharge or eventually destroy the capacitor. Most capacitors are designed with minimal size in mind, and often have very thin plates and electrical connections made of vacuum deposited metal. For this project, high current capacitors were chosen to facilitate rapid discharge.

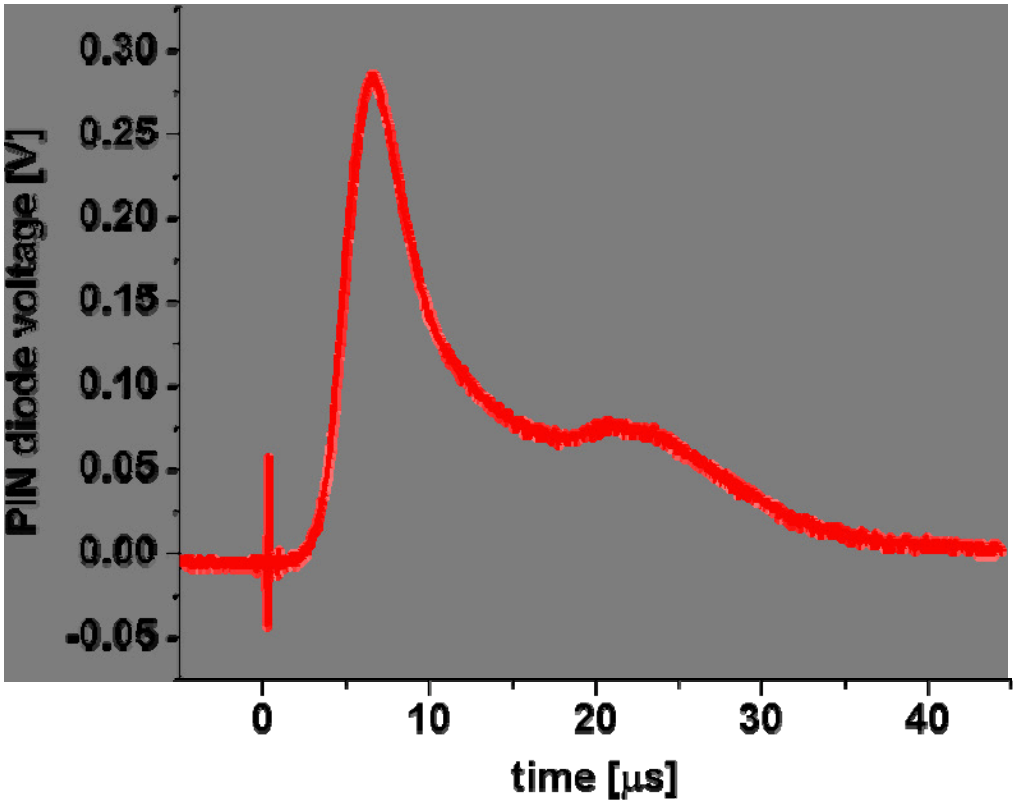

Figure 34 Relative Light Intensity vs. Time plot of flash operated at 900V, 2μF

The purpose of the trigger circuit is to provide the low current high voltage pulse initially needed to ionize the xenon gas and initiate discharge through the photoflash capacitor. In the trigger circuit, a voltage divider limits the maximum voltage across C6 to 300V (one-third of the total supply voltage). Capacitor C6 charges slowly through the 1MΩ resistor and primary coil of the trigger transformer. The rate of charging is too slow to induce a significant voltage on the secondary of the trigger transformer. The SCR T1 is normally non-conductive. However, when a 5V TTL pulse is administered to the gate, it goes into conduction and rapidly discharges C6. The rapid discharge of C6 causes an induced current in the secondary coil of the trigger coil TR1, which peaks at approximately 6kV. This voltage is significant enough to ionize the xenon gas in the flash tube and begin the flash.

System Performance

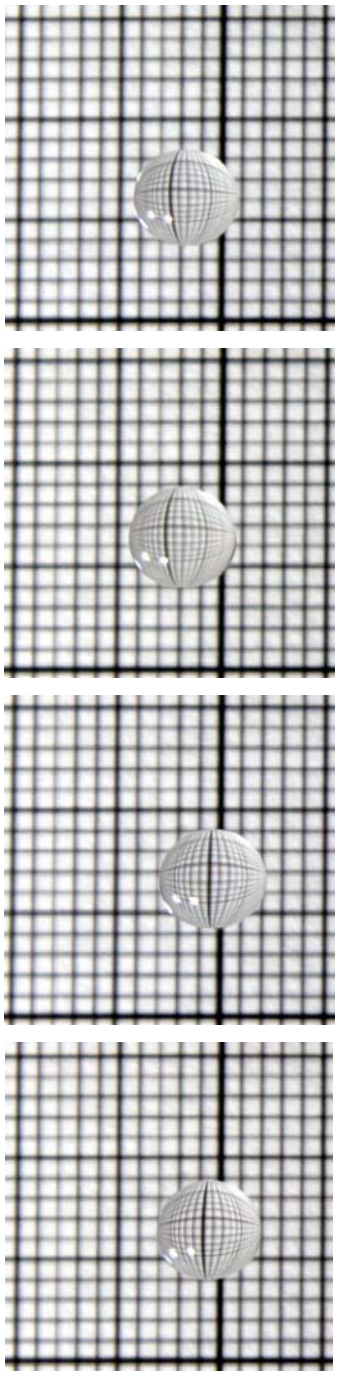

Figure 35 Consecutive shots of falling water droplet at a speed of 4.5m/s in front of a 1mm grid.

In order to verify the digital accuracy and performance of the system, quantitative shots were taken. The experimental setup for these shots was having a steady drip (one drop every two seconds) acting as the source. The water droplets started from a height of one meter and passed through a photogate and in front of a 1mm x 1mm grid. Using Newton's laws of motion, it was calculated that the water droplet velocity one meter below the drip source was about 4.7m/s. The water droplets fell approximately 1-2 cm in front of the paper grid and the camera lens was 20cm away from the paper in order to minimize the effects of parallax.

The consecutive photos in Figure 35 show water droplets taken from triggered shots with a delay of 114.3 ms. The system exhibits excellent repeatability. Any noticeable jitter in the height of the water droplets could be attributed to the drops not falling through the same position in the photogate beam created by the IR LED and IR phototransistor, which are both 5mm in diameter. Since the trigger is set to activate at partial beam obstruction, it is possible that water droplets falling through different parts of the beam could trigger the system at slightly different heights and cause a maximum jitter of approximately 2mm. However, these consecutive images show a jitter of less than 0.5mm, well within tolerance of the photogate.

In the future, a photogate will be constructed using rectangular LEDs and phototransistors to provide more planar beam that will trigger with less jitter.

Images

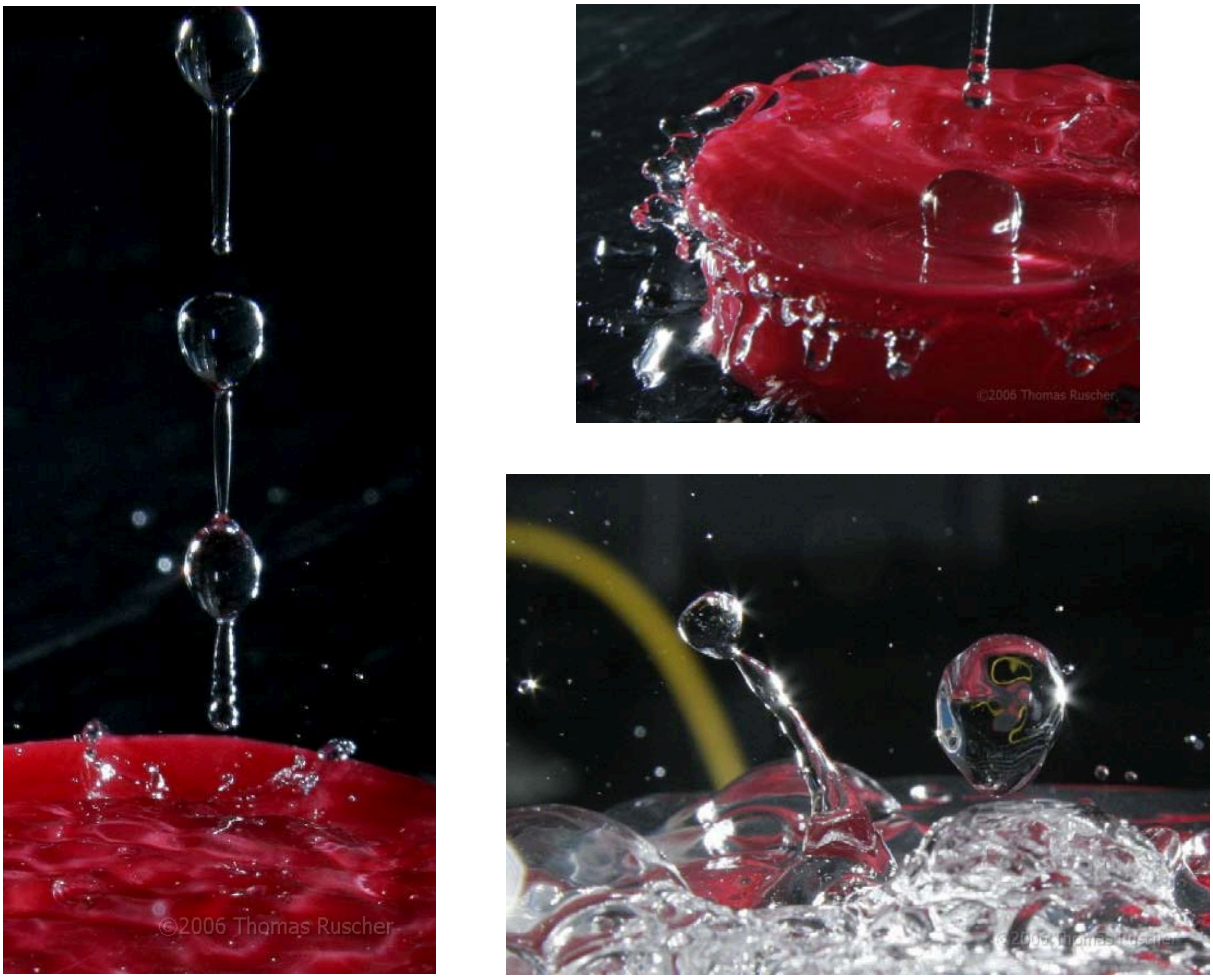

Figure 36 First untriggered images taken without the photogate trigger or the delay controller, just the high-speed flash. These, however, show the blur reduction from using a high-speed flash.

The images in Figure 36 are untriggered shots of water being poured from a height of 0.5m onto a red plastic cap and a beaker of water in the lower right hand corner. They were taken in the dark with the shutter on bulb, aperature set at f/8.0, and the high speed flash activated once.

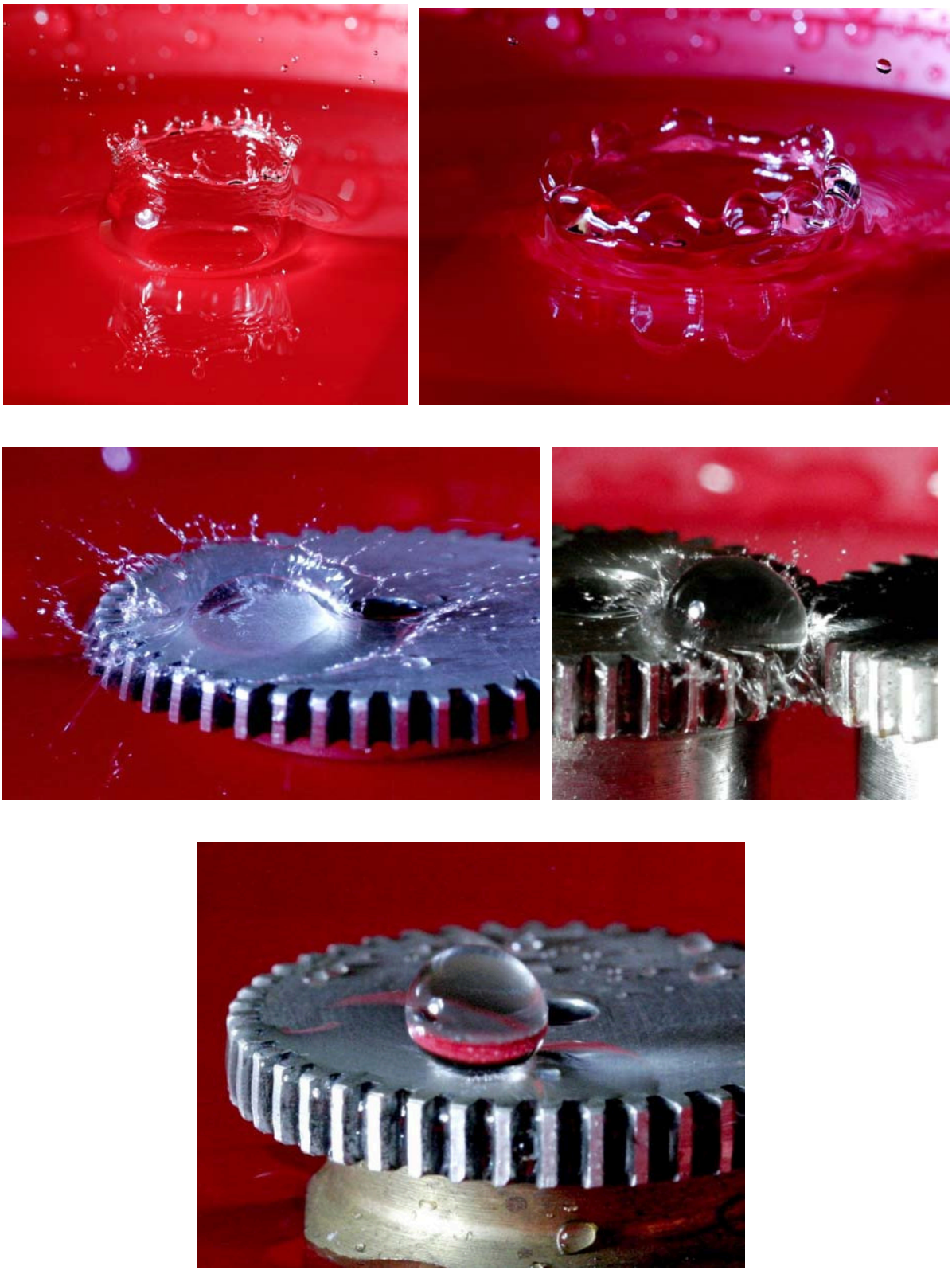

Figure 37 First triggered shots of water droplets using the completed photogate trigger, completed flashes, and the prototyped delay controller

The images in Figure 37 were the first triggered shots taken of water droplets. A steady drip source was set up using a water bottle suspended from the ceiling connected to 1/8" tubing with an in-line valve to control flow rate. The water droplets were allowed to fall approximately 1.5m through the photogate trigger mounted on the edge of a table into a large red plastic tray situated on a short stool. The delay was adjusted and programmed so that the flash would fire during water droplet impact.

These pictures, like the untriggered shots, were taken before the shutter synchronization feature was implemented in the system. Thus, they were taken with a bulb setting in the complete darkness. The camera was also set to an aperature of f/8.0 (found to be a good balance between depth of field and exposure).

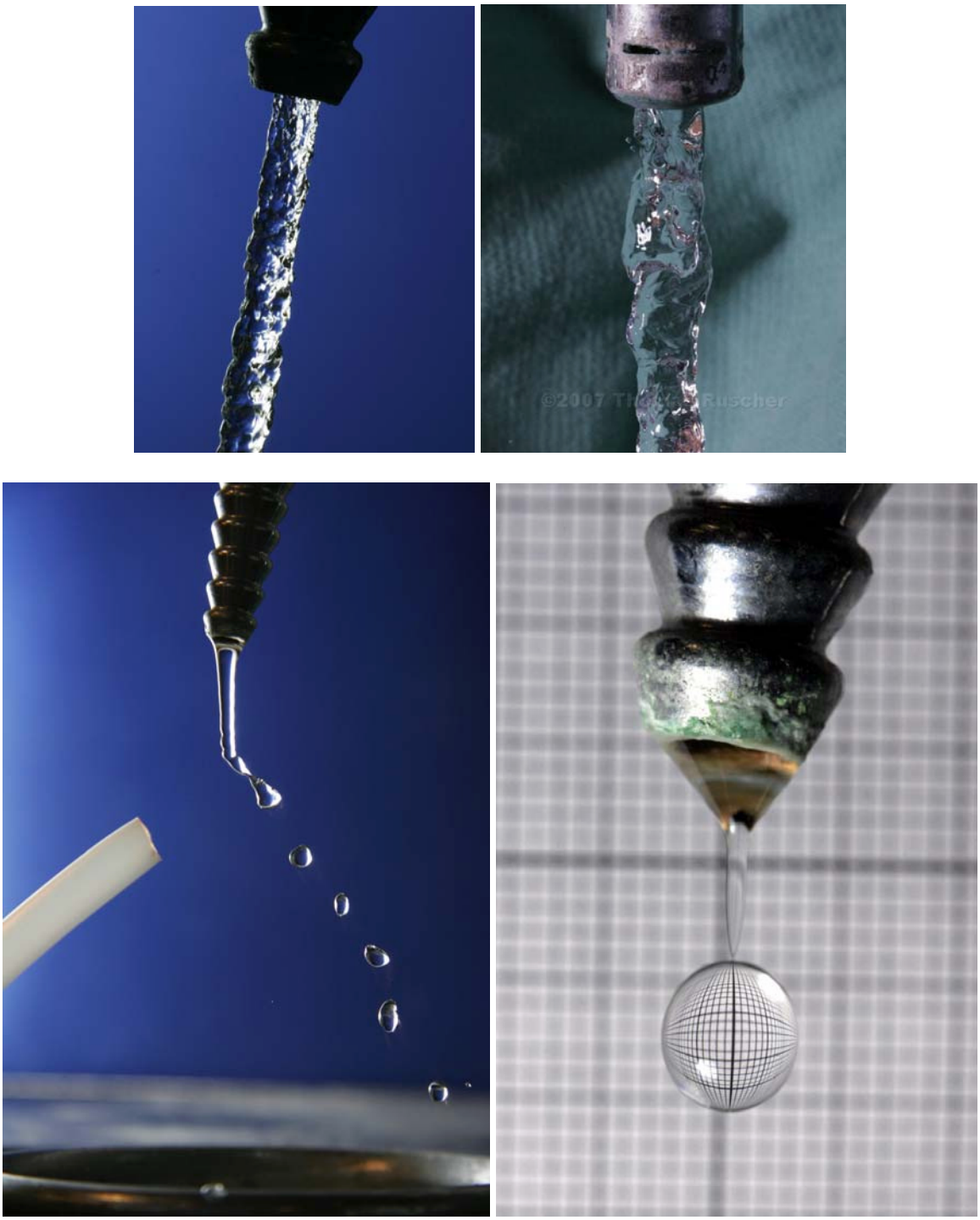

Figure 38 Shutter synchronized images taken in a lit room and captured with the completed high speed photography system.

The images in Figure 38 are the first pictures taken with the completed system, including the feature of shutter synchronization. They are mostly images of water droplets and streams

from a laboratory faucet. Some images, like washing the spoon and the razor, are presented here for their artistic merit.

Because these images were taken with shutter synchronization, they were taken in a lit room with a shutter speed of 1/200s that was synchronized to the firing of the high speed flash. Capturing these images was much easier without having to work in complete darkness. The aperature size was reduced from f/8.0 to f/11 in order to compensate for the extra light.

Conclusion

High-speed photography is an intersection of art and science. Both imagination and technical expertise are required to uncover images hidden by virtue of their transience. This project has been successful in creating a working digital high speed photography system consisting of a trigger, a delay controller, and high-speed flashes.

Now that all of the equipment has been designed and built, the future of this project will focus on the artistic potential in this system. One of the original intents of this project was to photograph rainstorms, to see what rain looks like when it impacts plants, the ground, and animals. As demonstrated by the images from the first three photo shoots, there is potential for a great deal of future photography with this system.

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