

DSP Project

Reminder: Project proposal is due Friday, October 19, 2012 by *5pm in my office (Small 239)*.

Budget: \$150 for project.

Free parts: Surplus parts from previous year's project are available on a first-come-first-serve basis in the lab room.

Analog ↔ Digital

As physicists, we know that:

- We live in an **analog** world of continuously varying signals.
- Almost all physical quantities (observables) are continuous in nature.

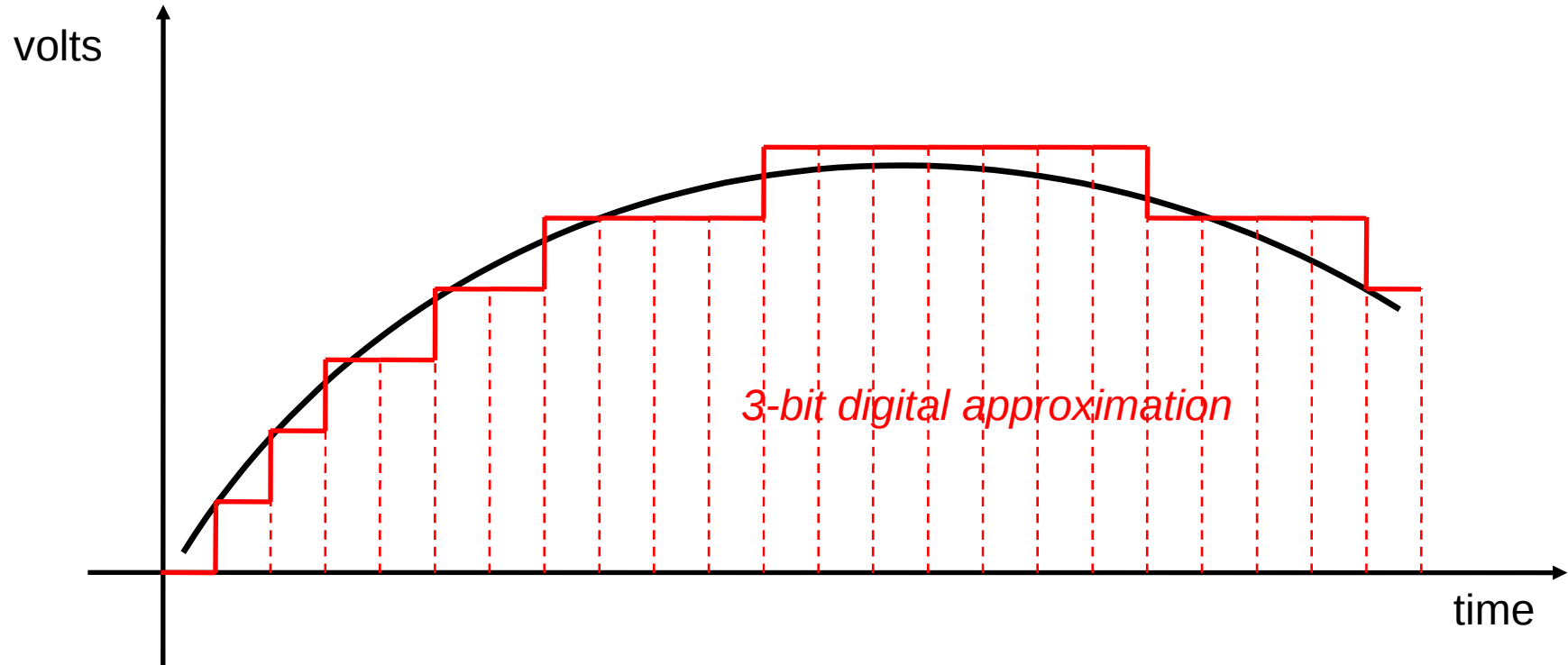
As electronics designers, we know that:

- Digital electronics is very **powerful**, **cheap**, and relatively **easy** to design (at least compared to analog circuits).
- Digital electronics only works with **digital signals**.

THEREFORE ...

If we're ever going to make anything useful, we need to find a way to convert (or approximate) an ANALOG signal to (by) a sequence of digital-binary numbers, and vice versa.

Analog → Digital



Algorithm: → At each clock cycle, round your analog voltage to the nearest digital value.

→ The size of a digital step is defined by $V_{\text{ref}}/2^n$ for an n-bit converter.

Shannon-Nyquist Sampling Theorem

THEOREM:

A continuous-time finite bandwidth signal can be exactly reconstructed from its samples if the sampling frequency is greater than 2 times the signal bandwidth B , where B is largest (non-zero) frequency component of the signal.

$F=2B$ is referred to as the Nyquist frequency (the lowest possible sampling frequency).

Practical Considerations:

- Any finite duration signal has $B \rightarrow +\infty$, so exact mathematical application of the theorem is impossible.
- The theorem indicates the frequency scale that one should use in order to usefully sample a signal → ***always use a sampling rate which is greater than twice the highest frequency component of “reasonable amplitude”.***

Flash ADCs

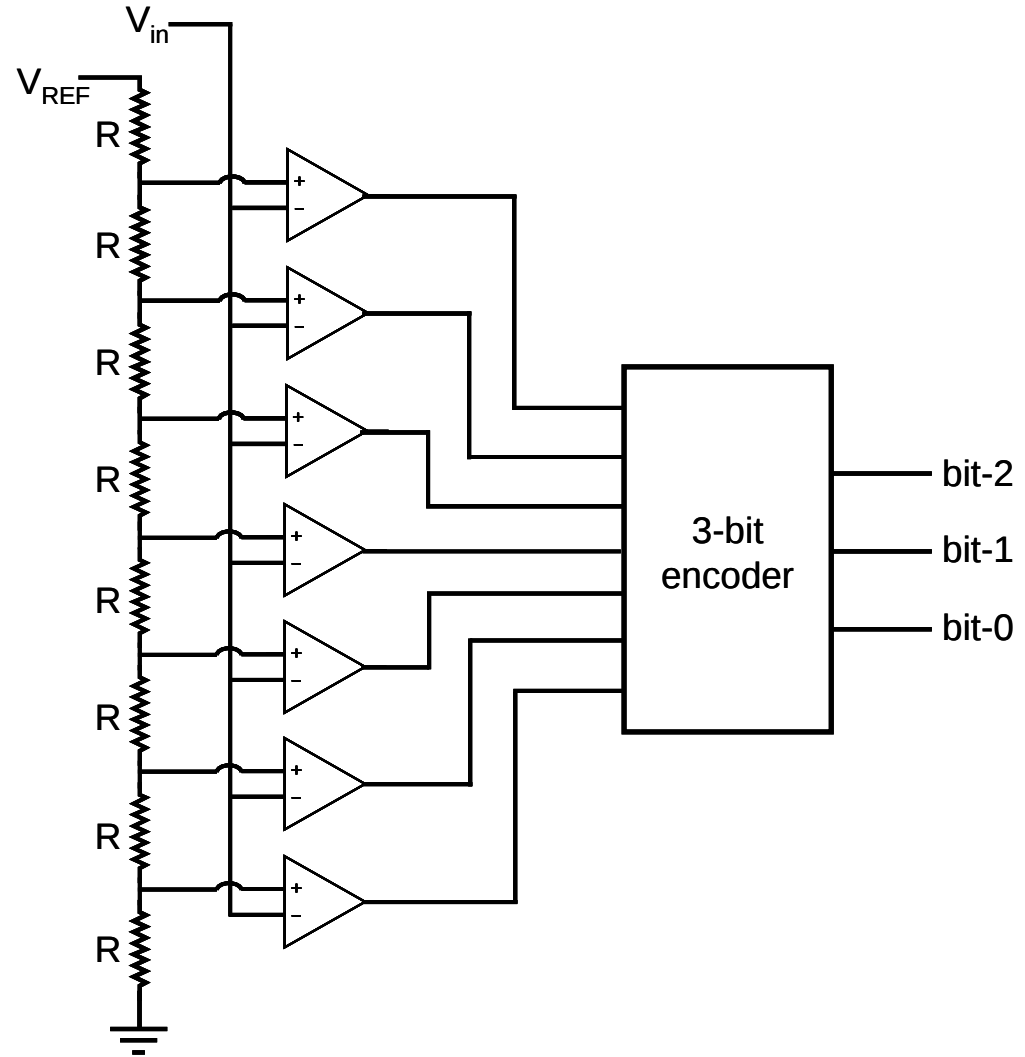
The fastest (and most expensive) n -bit ADCs use $2^n - 1$ comparators to determine which of the 2^n numbers the analog input is closest to.

8-bit ADC: 255 comparators.

12-bit ADC: 4096 comparators

In general, higher bit resolution results in a slower ADC (and more expensive).

Most digital oscilloscopes use an 8-bit ADC.

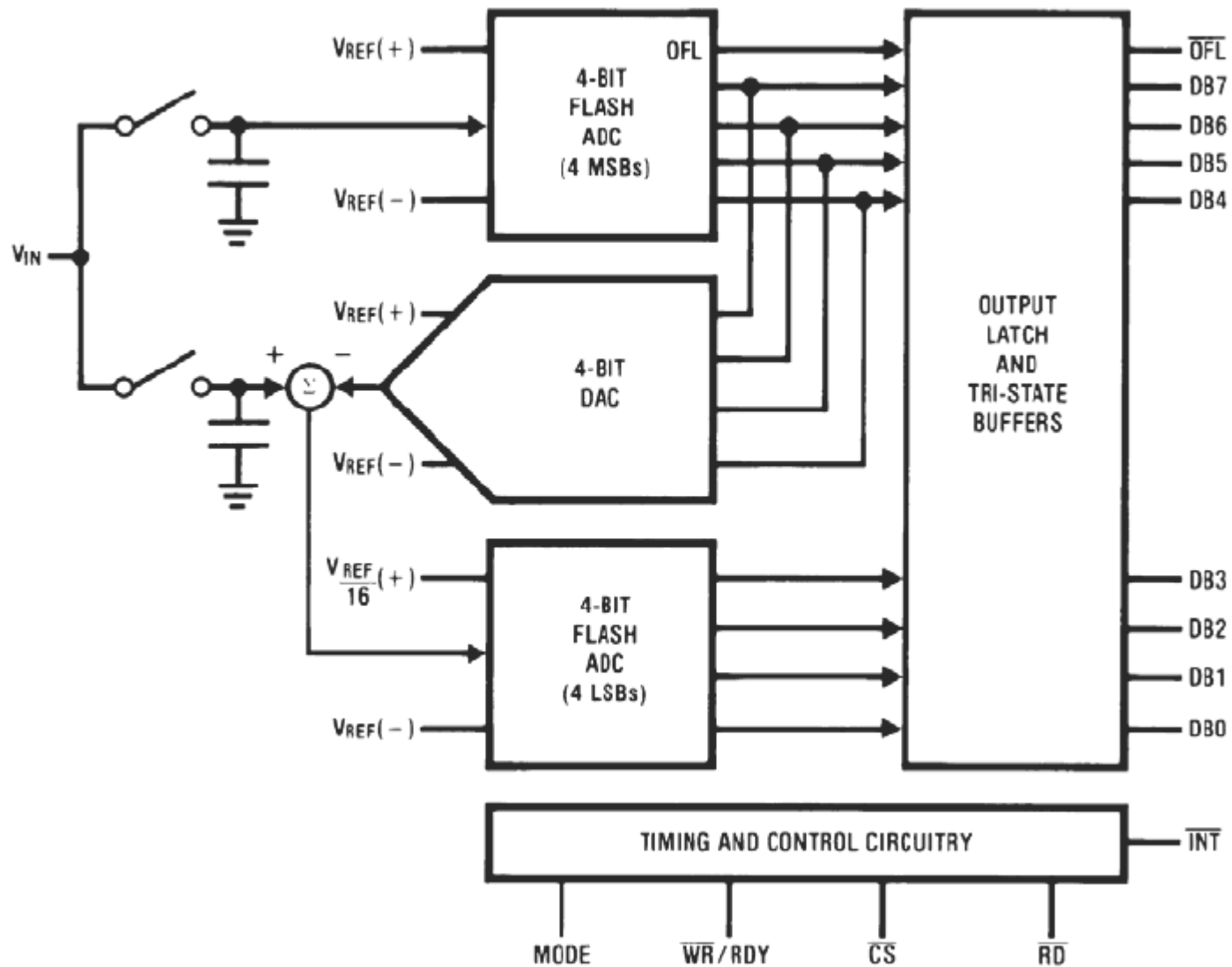


ADC0820 & TLC5510A: Half-Flash ADC (I)

- In order to keep the number of comparators small, it holds the input voltage, and converts it in steps:
 - Converts the upper four bits with a 4-bit ADC.
 - Converts the digitized value back into an analog value with a Digital-to-Analog Converter (DAC).
 - Subtracts this from the input to generate the smaller, difference voltage.
 - Finally, it uses a 2nd 4-bit ADC to convert the lower 4-bits.

- The entire process takes less than 800 ns when operating off the internal timing of the ADC0820 (RD mode) and about 150 ns for a TLC5510A (20 MHz clock).

ADC0820: Half-Flash ADC (II)



[figure from the National Semiconductor ADC0820 datasheet]

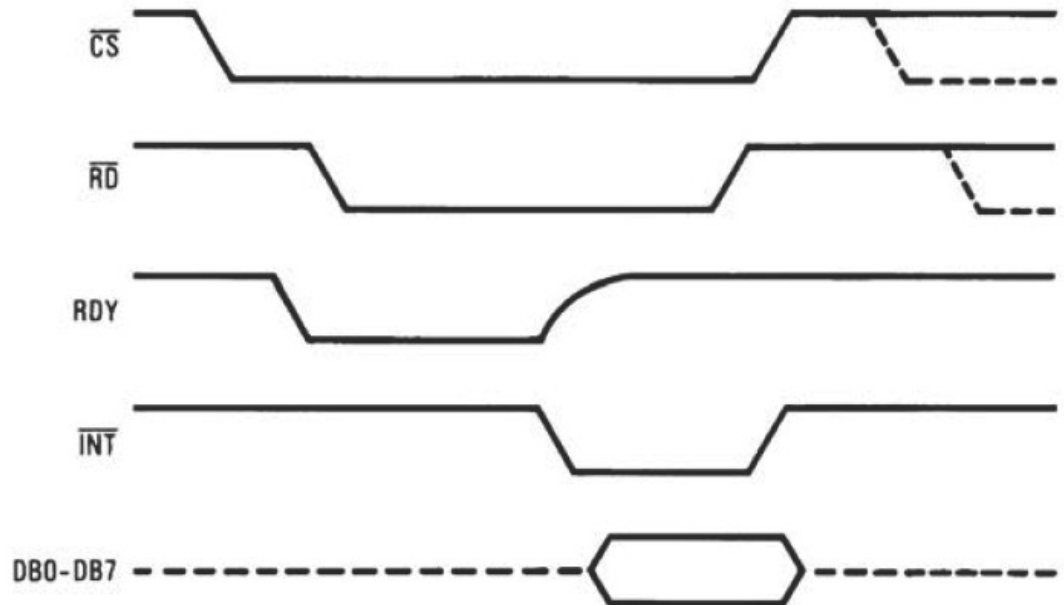
ADC0820: Half-Flash ADC (III)

Functional Table

Pin	Name	Function
1	VIN	Analog input; range $GND \leq V_{IN} \leq V_{CC}$
2-5	DB0-DB3	TRI-STATE data outputs; bit 0 (LSB) to bit 3
6	WR / RDY	WR-RD Mode - WR: With CS low, the conversion is started on the falling edge of WR. RD Mode - RDY: RDY will go low after the falling edge of CS; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch.
7	MODE	Select mode: LOW = RD Mode HIGH = WR-RD Mode
8	RD	WR-RD Mode With CS low, the TRI-STATE data outputs (DB0-DB7) will be activated when RD goes low. RD Mode With CS low, the conversion will start with RD going LOW; also RD will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and INT going low indicates the completion of the conversion.
9	INT	INT going LOW indicates that the conversion is completed and the data result is in the output latch. INT is reset by rising edge on RD or CS.
11	$V_{REF(-)}$	Bottom of resistor ladder; range: $GND \leq V_{REF(-)} \leq V_{REF(+)}$
12	$V_{REF(+)}$	Top of resistor ladder; range: $V_{REF(-)} \leq V_{REF(+)} \leq V_{CC}$
13	CS	CS must be low for the RD or WR to be recognized.
14-17	DB4-7	TRI-STATE data output—bits 4-7
18	OFL	Overflow—If the analog input is higher than the $V_{REF(+)}$, OFL will be LOW at the end of conversion. Can be used to cascade.

ADC0820: Half-Flash ADC (IV)

- In RD mode, the RD# line going LOW initiates the conversion.
- When the conversion is complete, the INT# line goes LOW & the data is latched into output buffers.
- The output buffers will be put in a Z state when WR# goes LOW until the INT# line goes LOW.

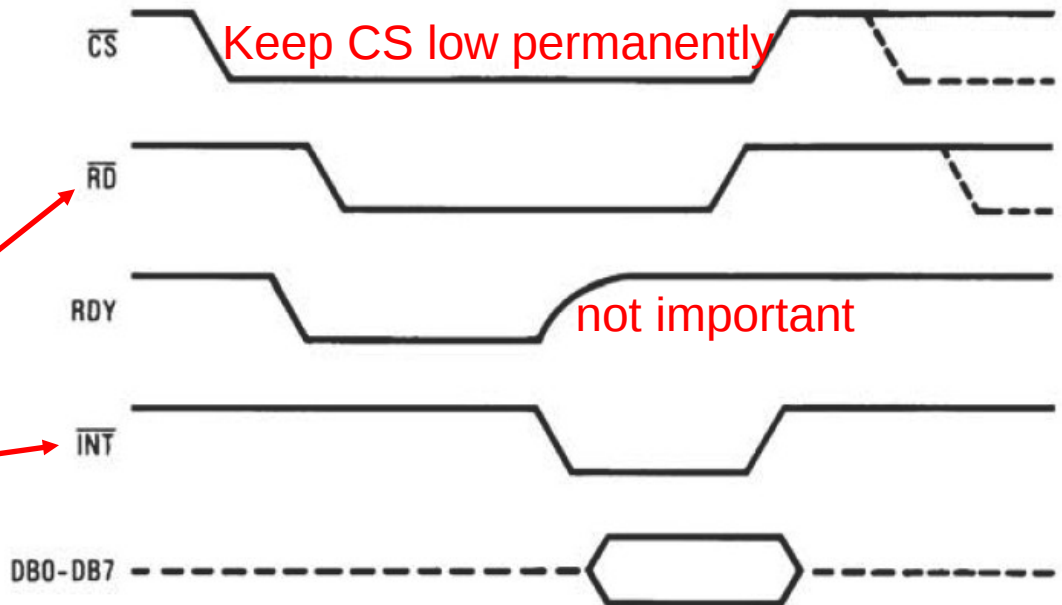


ADC0820: Half-Flash ADC (IV)

- In RD mode, the RD# line going LOW initiates the conversion.
- When the conversion is complete, the INT# line goes LOW & the data is latched into output buffers.

- The output buffers will be put in a Z state when WR# goes LOW until the INT# line goes LOW.

These lines are
IMPORTANT



TLC5510A: Basic Operation

\overline{OE}	1	24	DGND
DGND	2	23	REFB
D1(LSB)	3	22	REFBS
D2	4	21	AGND
D3	5	20	AGND
D4	6	19	ANALOG IN
D5	7	18	V _{DDA}
D6	8	17	REFT
D7	9	16	REFTS
D8(MSB)	10	15	V _{DDA}
V _{DDD}	11	14	V _{DDA}
CLK	12	13	V _{DDD}

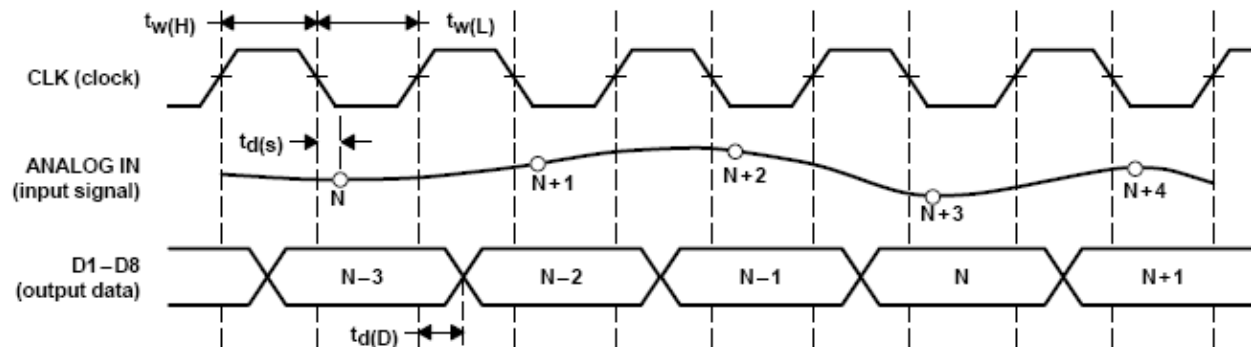


Figure 1. I/O Timing Diagram

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1 = LSB, D8 = MSB
\overline{OE}	1	I	Output enable. When \overline{OE} = low, data is enabled. When \overline{OE} = high, D1–D8 is in high-impedance state.
V _{DDA}	14, 15, 18		Analog supply voltage
V _{DDD}	11, 13		Digital supply voltage
REFB	23	I	Reference voltage in bottom
REFBS	22		Reference voltage in bottom. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFBS is shorted to REFB (see Figure 3). When using the TLC5510A, REFBS is connected to ground.
REFT	17	I	Reference voltage in top
REFTS	16		Reference voltage in top. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFTS is shorted to REFT (see Figure 3). When using the TLC5510A, REFTS is connected to V _{DDA} .

Mixed Signal Design

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the device.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are connected internally, the ground lead in must be kept as noise free as possible. A good method to use is twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts when additional logic devices are used. The AGND and DGND terminals of the device should be tied to the analog ground plane.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1- μ F and 0.01- μ F capacitors, respectively, and placed as close as possible to the affected device terminals. A ceramic-chip capacitor is recommended for the 0.01- μ F capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital ground terminals.
- V_{DDA} , AGND, and ANALOG IN should be shielded from the higher frequency terminals, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

Digital → Analog

A Digital-to-Analog Converter (DAC) is used to convert a digital signal into an analog voltage.

A DAC is useful for:

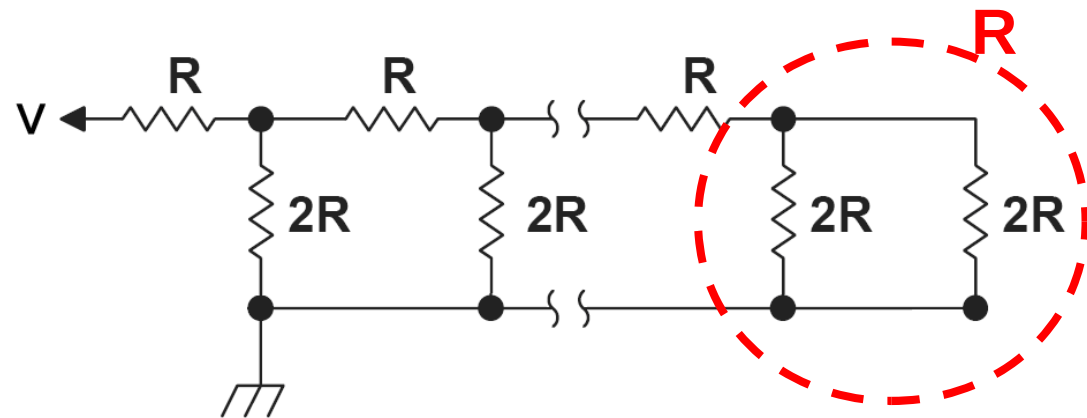
- Generating a voltage from a computer, microprocessor, or FPGA that will then control part of an experiment.
- Producing a digitally synthesized waveform (triangle, sine, or more complex).
- Converting digital music to sound, etc ...

(the CD standard is 16-bits at 44.1 KHz)

DACs are generally much faster than ADCs for a same bit resolution.

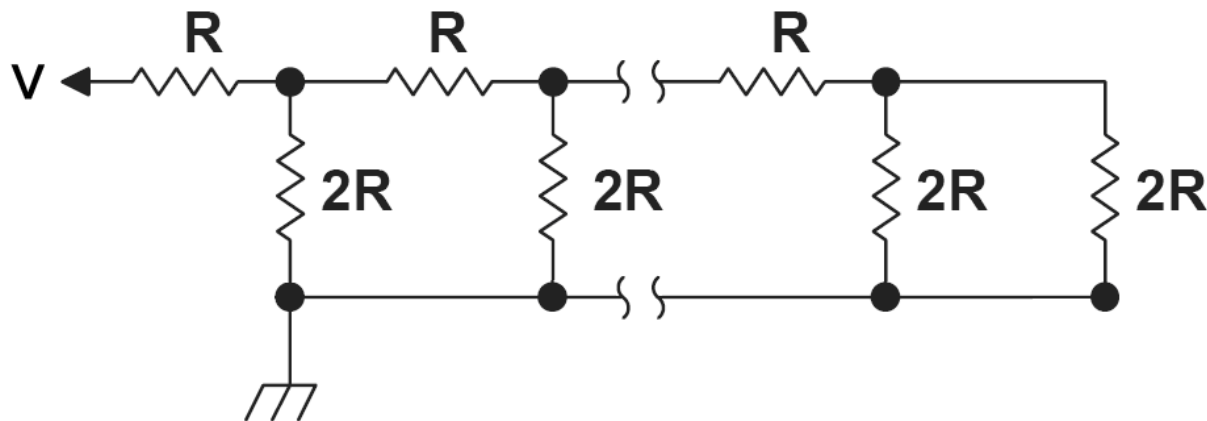
R-2R resistor ladder (I)

- It's easy to make the DAC output voltages.
- Look from the right-hand side
 - 2 parallel resistors
 - Each with a value of $2R$



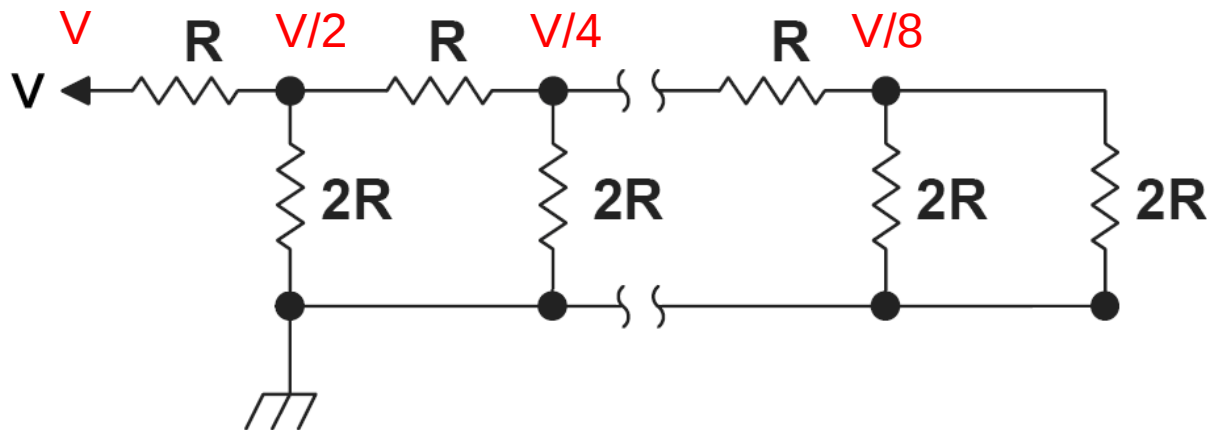
R-2R resistor ladder (II)

- Continuing farther to the left, we find that the effective resistance to ground is R at every dot on the top line



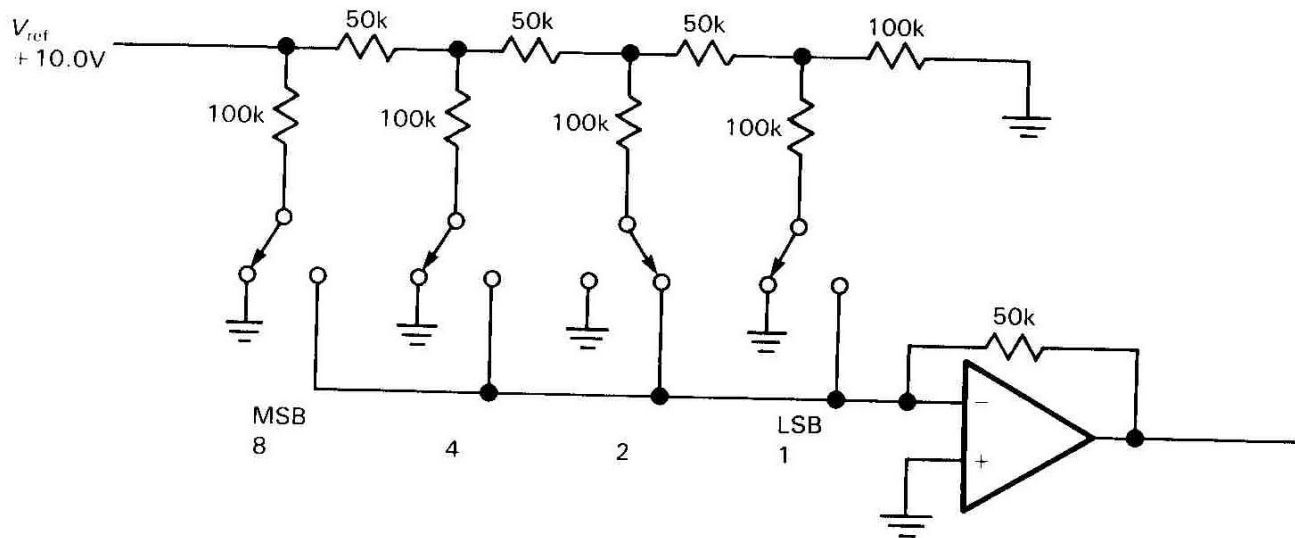
R-2R resistor ladder (III)

- The ladder acts like a series of voltage dividers that reduces the voltage by an additional factor of 2 at each R - $2R$ junction.
- V decreases by half at each connection point along the top rail.
- Thus each output voltage is related to the input voltage by a power of two.



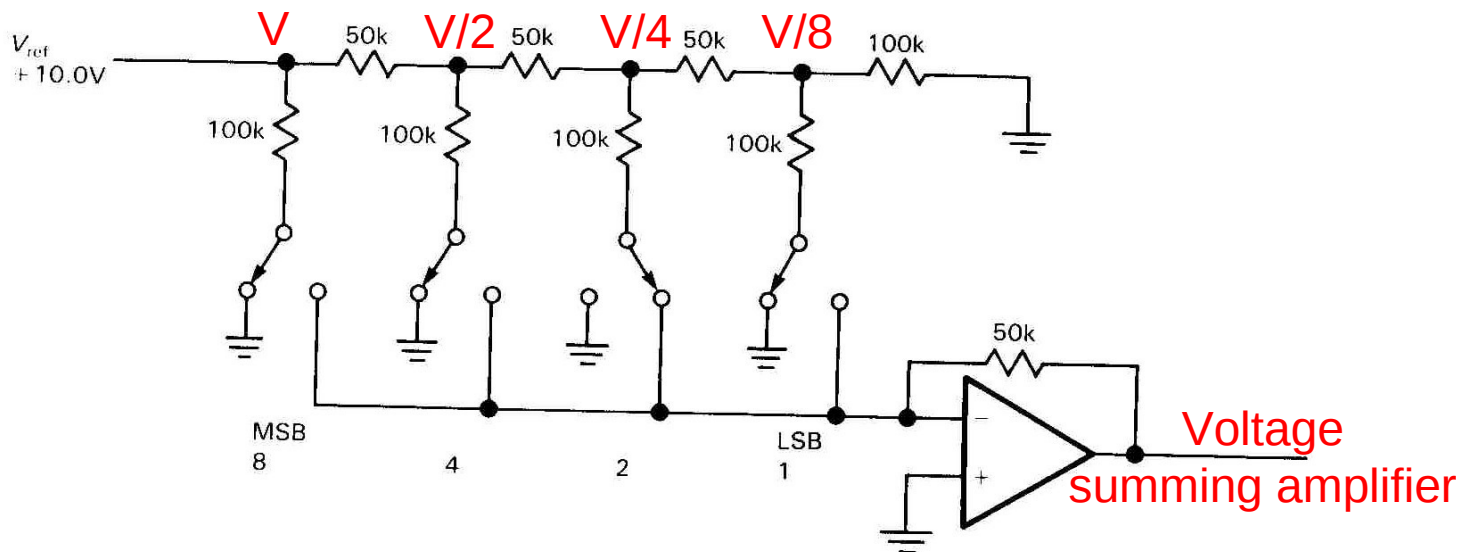
Simple DAC

- We can generate an analog voltage by adding together the voltages represented by the various stages in the ladder.
- If we sum the ladder outputs based on a simple a binary representation in switches then we have a DAC.



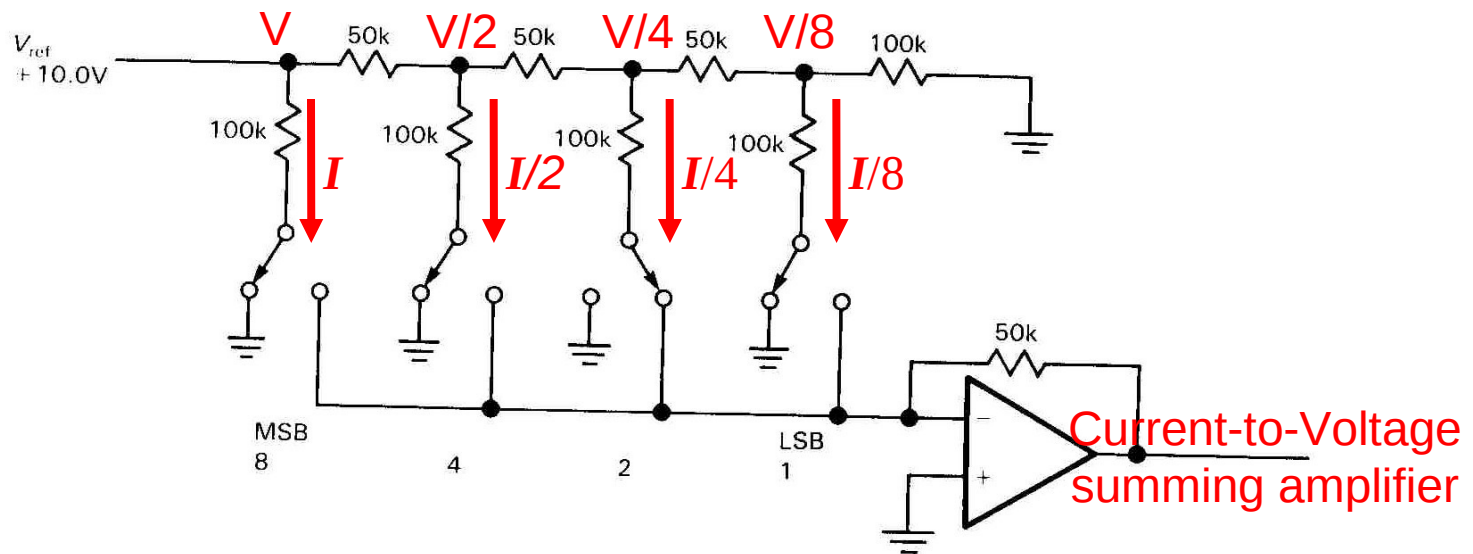
Simple DAC

- We can generate an analog voltage by adding together the voltages represented by the various stages in the ladder.
- If we sum the ladder outputs based on a simple a binary representation in switches then we have a DAC.

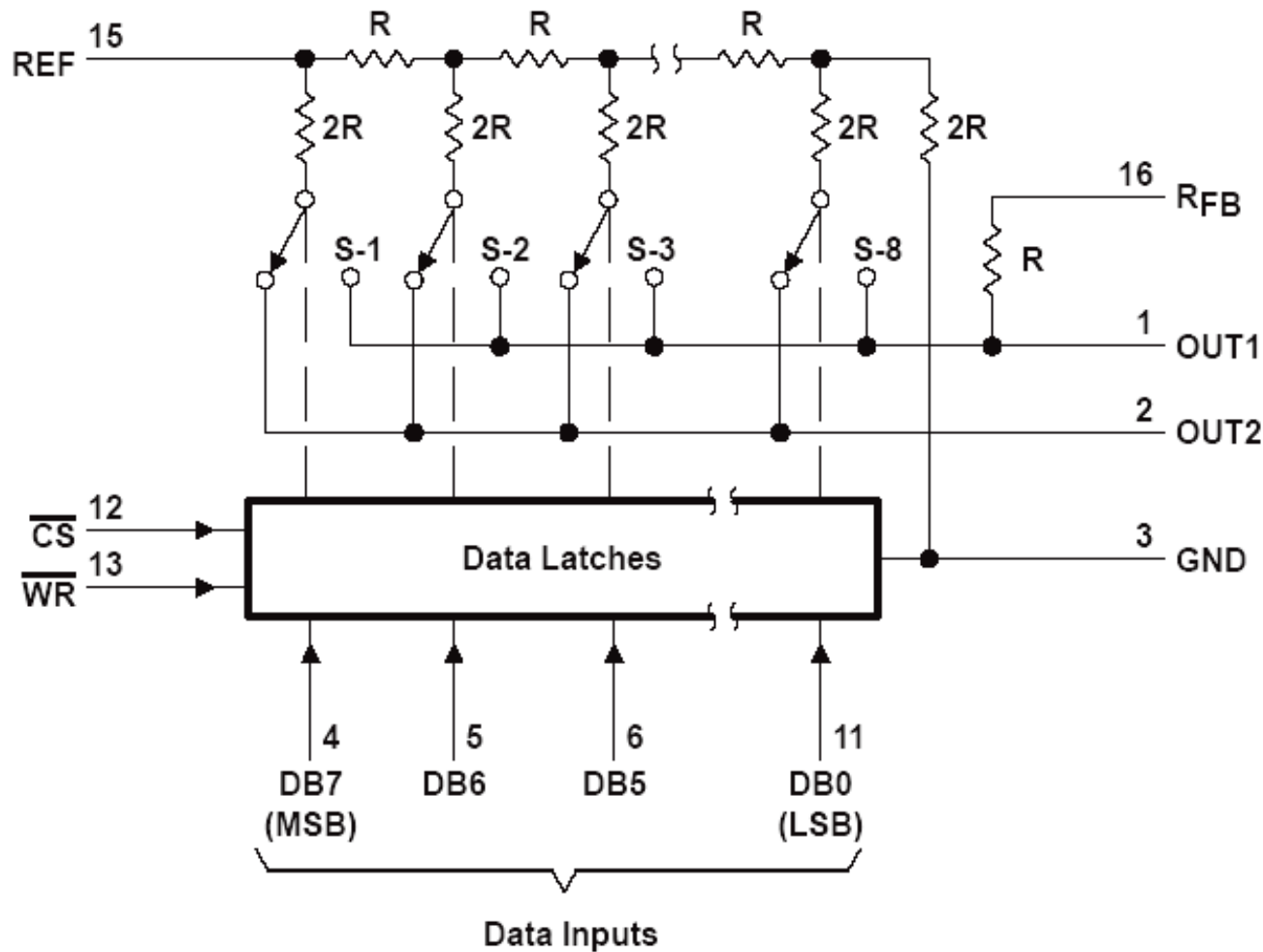


Simple DAC

- We can generate an analog voltage by adding together the voltages represented by the various stages in the ladder.
- If we sum the ladder outputs based on a simple a binary representation in switches then we have a DAC.



A real DAC: the TLC7524

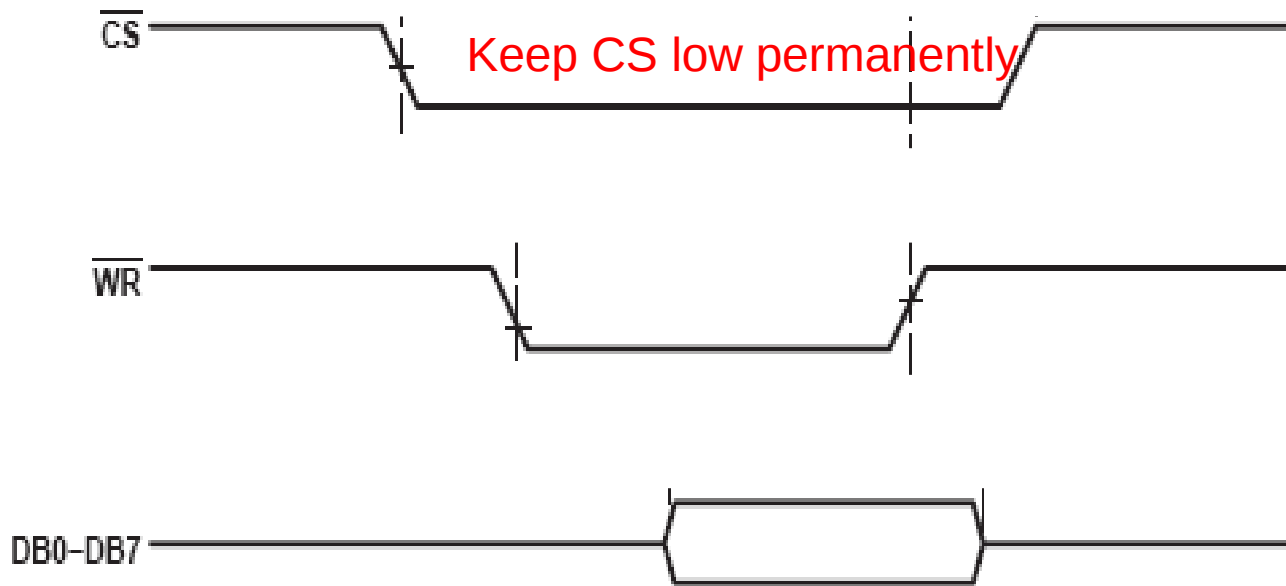


DAC (TLC7524)

[figure from Texas Instruments TLC7524 datasheet]

TLC7524 timing

- The data on the digital inputs is sent to the analog output when WR goes LOW.
- When WR is HIGH, the digital inputs and analog output remain latched to their present values.



[figure from Texas Instruments TLC7524 datasheet]

Lab 6: ADCs and DACs

Analog to Digital and back to Analog

