Electronics II
Physics 351 (CRN 14200/14201)
Fall 2012

Lecture: M 2:00-2:50 Small 233
Lab: T 2:00 - 4:50 or W 2:00 - 4:50 Small 230

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Course Objectives and Topics: The primary purpose of this course is to teach you how to design both basic and advanced digital electronic circuits for digital logic, signal acquisition, and digital signal processing. Topics that will be covered include:

- Binary numbers, logic gates, and Karnaugh maps
- Memory, flip-flops, and clocked latches
- Clocks, timing, and one-shots.
- Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC).
- Field Programmable Gate Arrays (FPGA) and Verilog language FPGA programming.

Class Structure: The class hours are divided into two parts: Lecture and Lab. The lecture will be on Monday 2:00-2:50 pm in Small 233, and will cover the concepts to be covered in the lab later in the week. The lab portion of the class will be held on Tuesday 2:00-4:50 pm or Wednesday 2:00-4:50pm. You will have access to the lab at times other than the scheduled time. Many labs will include a design component. The designs should be prepared prior to attending lab so the lab measurements can be finished on time. Many designs can be prepared and refined using the Quartus II software.

There is no official textbook for the course. I will be posting introductory chapters and laboratories created specifically for the course on the website before the lecture. These chapters and labs were originally created by Prof. Jeff Nelson and Prof. Bill Cooke and have been adapted to the current course. While there are many good electronics textbooks, I recommend that you consult the following book for design tips and concepts: The Art of Electronics (2nd Edition, 1989-1999) by P. Horowitz and W. Hill. It is available in the Physics Library under call number TK7815 .H67 1989.

There is no final for this course.

Grade: Your final grade for the course will be determined with the following weight:

Notebooks	40%
Participation:	10%
Project:	50%

Notebooks: Your lab book should be a composition style notebook with either line or quadrangle ruling or a computation logbook. It can be obtained at most stationary stores (i.e. campus bookstore, Staples etc) Your lab book is the primary record of your work and data. You should record everything that you do in the lab book, so that anyone (such as the instructors and yourself) can understand what you have done and measured. You should include circuit diagrams, observations, questions, answers, design considerations, measurement data, and analysis. Diagrams, data, graphs, and other notes on separate pieces of paper should be glued, taped, or stapled into the lab book. As a general rule, you cannot write too much down. The lab book will be graded primarily on completeness and to a lesser extent on neatness (i.e. better to be complete than neat, though doing both is better yet). It should also feature a table of contents. The lab books will be turned in every weeks and returned before the next lab.

You should enter you lab notes and data directly into the lab book. A 'scratch' lab book that is neatly copied into the lab book at a later time is not appropriate and will result in a significantly reduced participation grade.

Field Programmable Gate Arrays: Field Programmable Gate Arrays (FPGAs), are a type of programmable logic chip in which complex digital circuits can be programmed into a chip: the thousands of logic gates inside the chip are hard-wired to provide a compact and reliable digital circuit.

The course will use the Quartus II FPGA programming software by Altera Inc, an industry standard for FPGA programming. The software package can be used to program FPGAs and to simulate almost any type of digital circuit. Advanced FPGA programming will involve the Verilog programming language which is include in the Quartus II software package. The software is available on the electronics lab computers (Small 230).

Project: The design project is the most important part of the course. More details of the project will be announced in the first few weeks of class. The project will be graded as follows:

Formal project proposal	10%
Device construction	15%
Device performance	15%
Web presentation of device	5%
Project lab book	5%
Total	50%

Weekly Schedule:

Topic	**Week**
No Class Partial Week	August 29-31
Digital Logic	September 3-7
Introduction to FPGAs	September 10-14
Memory	September 17-21
Timing	September 24-28
Counters and Registers	October 1-5
Analog-Digital Interfacing	October 8-12
No Class Fall Break	October 15-19
Project proposals due	**5pm October 19**
Project	October 22-26
Project	October 29 - November 2
Project	November 5-9
Project	November 12-13
No Class Thanksgiving	November 19-23
Project	November 29-30
Project Reports	December 3-7